PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G01R 31/08, H04H 27/10, H04L 27/10, 27/18, 5/16

A1

(11) International Publication Number: WO 98/59254

(43) International Publication Date: 30 December 1998 (30.12.98)

(21) International Application Number: PCT/US98/11107

(22) International Filing Date: 1 June 1998 (01.06.98)

(30) Priority Data:
08/881,481 24 June 1997 (24.06.97) US

(71) Applicant: INTELOGIS, INC. [US/US]; Suite 108, 12257 Business Park Drive, Draper, UT 84020 (US).

(72) Inventors: SCHURIG, Alma, K.; 1175 E. 1220 N., Orem, UT 84097 (US). BUTLER, Kent, A.; 3688 North Fillmore Street, Cedar Fort, UT 84013 (US). HAAB, Daniel, B.; 948 South 2350 East, Springville, UT 84663 (US). PHILLIPS, David, P.; 395 N. Palisade Drive, Orem, UT 84097 (US).

(74) Agent: ALTMAN, Daniel, E.; Knobbe, Martens, Olson and Bear, LLP, 16th floor, 620 Newport Center Drive, Newport Beach, CA 92660 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: IMPROVED UNIVERSAL LAN POWER LINE CARRIER REPEATER SYSTEM AND METHOD

(57) Abstract

An improved local area network (LAN) to power line carrier (PLC) interface and protocol using FSK is described. This system provides improved data symmetry, higher data rates, lower bit error rates, improved synchronization and alignment of data, as well as improved carrier detection. The system provides high speed frequency shift key (FSK) modulation over the power line to achieve high data rates. Performance may be further improved by using a novel combination of FSK modulation and differential shift key (DFSK) modulation to provide an improved local area network (LAN) to power line carrier (PLC) interface and protocol using FSK and DFSK. DFSK is described and shown to provide improvements in the modulation and demodulation of data transferred over digital networks.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania
AM	Armenia
AT	Austria
AU	Australia
AZ	Azerbaijan
BA	Bosnia and Herzegovina
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CU	Cuba
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GH	Ghana
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IL	Israel
IS	Iceland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgyzstan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakstan
LC	Saint Lucia
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LS	Lesotho
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
MK	The former Yugoslav Republic of Macedonia
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TM	Turkmenistan
TR	Turkey
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam
YU	Yugoslavia
ZW	Zimbabwe

IMPROVED UNIVERSAL LAN POWER LINE CARRIER REPEATER SYSTEM AND METHOD

Background of the Invention

Field of the Invention

This invention relates to Power Line Carrier (PLC) Local Area Network (LAN) repeaters in which LAN signal/data are transferred over the existing power lines of a building via power line carrier rather than through special cables which must be installed professionally. A PLC LAN repeater must (a) interface effectively with the LAN and its protocols, (b) achieve data rates over the power lines which are at least an order of magnitude faster than those of prior art PLC systems and (c) provide acceptable operation to a plurality of users. While many LAN (including Arcnet, Token Ring and RS-485) are in use and may be serviced by the instant invention, the Ethernet LAN will be examined to illustrate the interface and data rate requirements for this invention.

More specifically, this invention relates to systems for PLC LAN repeaters which employ a differential frequency shift key (DFSK) technique to increase data rates and noise immunity and system reliability. The use of DFSK technology improves the performance of PLC LAN repeaters by improving edge resolution; reducing the effective bandwidth requirements of the transmitted signal, thereby permitting increased data rate or narrower filter bandwidth; reducing the temperature coefficient and tuning requirements by AC coupling of the analog data; reducing startup transients in the data slicer; rejecting noise on the marking frequency; permitting special characters for compression or control purposes. This invention incorporates a number of other improvements over the existing technology, including: improved RF and IF filters to increase the data rate; synchronization of the data rate clock with the carrier frequency; a realignment bit every ninth bit; a group knowledge (ACK) which is frequency shift keyed (FSK) at a lower data rate; and carrier detection is accomplished without use of a Receive Signal Strength Indicator (RSSI), using special preamble and start characters. These improvements provide a complete modulation and demodulation system for PLC with significantly enhanced data quality.

Description of Related Art

The Ethernet IEEE 802.3 standard provides for mechanical and electrical standards and protocols for multiple users to share ("network") data transfer access to a common transmission medium or bus (the "ether" of a cable) but still maintain acceptable data access times and transmission rates. A user accesses the network through his node on the network, which is usually his computer/workstation with a hardware LAN interface physically connected to the network cable as the node. Proprietary network software (such as NetWare and Windows for Workgroups) runs with the workstation's operating system to manage the interface between the user's applications and the network. Individual users are provided unique ID/address codes so that only messages with the correct address preamble may be accepted and routed into their node/workstation while ignoring all others. The protocols also provide for detecting and managing collisions between the plurality of network users seeking simultaneous access to the network so that only one user may safely transmit data at a time. The software for implementing this Carrier Sense Multiple Access with Collision Detection protocol (CSMA/CD) is usually divided between firm embedded in the Ethernet interface cards and the proprietary workstation software.

IN a peer-to-peer network configuration, two or more workstations may be networked together. Each user may communicate with any other user with network protocols arbitrating data collisions when more than one user seeks to initiate communication at a time. In the Ethernet specification, when a collision is detected, each user interface backs off for a "random" time before reattempting access (CSMA/CD). In a client-file server configuration, each user communicates with the server as well as directly with other users. Arbitration takes place between the users and the server.

Since a large number of users results in frequent data transfers as well as collision arbitration, the data rate of Ethernet must be very high to accommodate acceptable transmission time delays. Consequently, the IEEE 802.3 standard provides for data transmission at the rate of 10Mbps in packets of no more than 1,500 bytes. Such speeds are three orders of magnitude beyond prior art PLC data communication/LAN technology.

In addition, Ethernet mechanical standards provide for bidirectional communications either by coaxial cable ("thin/thick net") or by dual sets of Unshielded Twisted Pairs (one for each direction of data flow) called UTP or "10baseT" cable. Coaxial interfaces utilize a transceiver to interface between the bidirectional digital data of one computer and the RF data modulated signals of the coax/thin net. The 10BaseT medium accommodates the bidirectional data more directly by using 2 sets of twisted pairs (one for transmit and one for receive data). To achieve 10Mbps data throughput an interface standard similar to RS-485 (CCITT V.11) is employed, which provides for balanced, isolated and low impedance transmitters and differential receivers. The RS-485 standard provides for up to 32 transmitters and receivers networked on the same data line. Both coaxial and UTP communications interfaces/LAN cards have been reduced to low cost, high performance commercial products sourced by many companies.

The problem with LAN systems such as Ethernet is the installation expense for the cables which can exceed $100 per "node" or user. Often the old commercial structures are prohibitively difficult to retrofit. Other companies are periodically requiring reconfiguration of office space to accommodate changing commercial needs and require a less expensive and more friendly method for connecting and reconfiguring workstations to their LAN. And there are limitations as to the length of cable one can use. The instant invention provides a cost effective alternative to special cable installation by "repeating" the network via power line carrier data transmission over the AC power lines of a premises.

RF LAN repeaters have been offered in the 900 MHz range where sufficient bandwidth is available to transmit the 10Mbps signals. However, the 900 MHz systems are not only prohibitively expensive (at $600-800 per node) but also exhibit propagation problems and interference in commercial buildings where LAN systems are most commonly used and the software for managing a large number of users has been unacceptable, which (in addition to high cost) has detracted seriously from their widespread proliferation.

Summary of the Invention

The instant invention, however, provides both the interface for the commercial LAN card/port as well as the PLC repeater system capable of transferring data packets at sufficiently high rates and with collision

detection/prevention firmware for transparency with respect to small and medium sized LAN systems at a competitive cost.

The PLC repeater/transreceiver comprises both a novel data transmitter and advanced data receiver with over 90 dB of gain, which together are capable of high bandwidth/data rate Frequency Shift Key (FSK) transmission data rates of DC to over 2 Mbps (million bits per second). RF PLC frequencies of 2-20 MHz combined with sufficient transmitter power and receiver sensitivity achieve adequate signal to noise ratios in AC power systems with high attenuation and noise. The over-90 dB sensitivity/RF range permits proper data transmission over the 3-phase power distribution system in industrial installations with capacitive loads and electrical equipment induced noise. The RF carrier frequencies in combination with the receiver sensitivity permit the signals to jump phases in residential 2-phase and industrial 3-phase distribution systems by means of the capacitance between phases in the wiring. The highly deviated (greater than 100kHz) FSK signal in combination with the high RF carrier frequency and 3 stages of RF and IF filtering in the receiver makes the data transmission very robust in the presence of electrical interference.

Multiple transceivers are capable of simultaneous operation at different RF carrier frequencies, permitting full duplex serial communication as well as multiple networks operating without interference on the same power line bus.

The LAN interface comprises 2 subsystems: (1) a bidirectional LAN card or port interface (a) for receiving (and storing in buffers) outgoing data packets in the LAN system format from a user's workstation for transmission to other LAN users and (b) for returning data packets in the LAN format to the same workstation card/port from other users, and (2) an asynchronous serial data transceiver (with data buffering) which (a) drives the PLC data transmitter with the outgoing data packets stored in the buffer by the port interface and (b) receives incoming data from the PLC data receiver originating from other users. The serial data transceiver is controlled by a system controller with firmware (i) to arbitrate collisions on the power line data bus with other users and (ii) to manage the bidirectional transfer of data packets: OUTGOING from LAN interface to serial data transceiver and INCOMING from serial data transceiver back to LAN interface. Commercial controllers are available for managing the entire repeater which contain both the asynchronous PLC serial port and some LAN interface ports such as RS-232 and RS-485, as well as parallel ports.

A relatively simple and low cost PLC LAN repeater networks workstations through their standard serial ports using software such as NetWare Lite. The PLC LAN repeater consists of a low cost but competent microcontroller with (1) an RS-232D port (115.2Kbaud) for connecting a built-in serial port to the users and (2) an asynchronous serial communications port which connects to the PLC transceiver. The onboard controller firmware manages the storage and retransmission of data packets in addition to collision arbitration and detection on the PLC bus. The PLC LAN repeater thus converts a two-user RS-232 peer-to-peer network into a more-than-two user network (like RS-485) without the user having to by a (more expensive and less common) RS-485 type of interface. The data rate for PLC bus could be 10 times higher than the limited 115.2 Kbaud of the conventional serial port, making this kind of PLC bus network capable of handling much larger data traffic than is possible with an ordinary RS-232 serial port network.

Alternatively, personal computers (PCs), printers and other electronic devices can be networked together using this invention through standard parallel ports using standard interface protocol software and controllers, including but not limited to Windows 95.

The proliferation of embedded controllers in a plethora of electrical/electronic equipment can be effectively networked with control maintenance/security systems via PLC LAN repeater subsystems also embedded in the equipment, which repeaters network the serial port of the embedded controllers to a PLC LAN bus via the existing power cord of the equipment and the power distribution system of a premises. The inventors have applied this same concept of embedded PLC LAN repeater to many types of computers and related products, modems, industrial control systems and utility metering equipment. The instant invention facilitates the higher data rates and transmission integrity required by these systems.

For LANs using the RS-485 ports, a high-speed 485 interface is provided together with a controller for converting the data to PLC transceiver compatible rates and format.

A more complex configuration for Ethernet illustrates the scope of application of the universal repeater and utilizes a commercial Ethernet interface chip in combination with a microcontroller with global high-speed communications port for servicing the PLC transceiver. This provides a transparent PLC repeater which connects to the standard Ethernet ports of a workstation and, with NO additional software or hardware, permits multiple users to network over the existing power lines of a premises.

The versatility of configurations also supports Token Ring and Arcnet protocols, chiefly because the PLC transceiver is competent enough to handle sufficiently high data rates to permit transparent operation for smaller segments of the network.

Objects

Accordingly, it is an object of the invention to provide an advanced method and system of high data rate power line carrier transmission which supports the data rates required by local area networks.

It is an object to provide a method and system of interfacing power line carrier repeaters with conventional network cables or cards to convert LAN data to PLC repeater acceptable data and to convert PLC repeater data to LAN data.

It is a further object to provide a method and system of arbitrating multiple PLC LAN repeaters to permit efficient and exclusive access to a particular frequency/channel of the power line medium.

It is an object to provide a PLC transceiver which sends data with a bandwidth of DC to over 2 Mbps and which is therefore able to transfer wideband analog signals/data of DC to over 1 MHz bandwidth.

It is an object to provide an embedded PLC network repeater system capable of being interfaced with embedded controllers in equipment for networking said equipment with automation, control and diagnostics systems and general network services.

It is a further object of this invention to provide an embedded PLC network repeater system having an improved modulation technique, known as Differential Frequency Shift Key (DFSK) in conjunction with Frequency Shift Key (FSK) which is able to trigger data state changes with much improved resolution.

A still further object of this invention is to provide an embedded PLC network repeater system having a DFSK modulation technique which by centering more energy around the carrier frequency minimizes the effective bandwidth required for a given data rate.

A further object of this invention is to provide an embedded PLC network repeater system employing improved RF and IF filters to provide wider and flatter pass bands while maintaining system data reliability with changing data compositions.

Another object of this invention is to provide an embedded PLC network repeater system employing a realignment bit at the end of each data byte to aid the re-synchronization of the receiver, thereby permitting increased data rates.

Another object of this invention is to provide an embedded PLC network repeater system with improved carrier detection and acknowledgment techniques.

An additional object of this invention is to provide an improved modulation and demodulation technique, known as Differential Frequency Shift Key (DFSK), for all networking media or electronic communications systems, including RF and wired media.

Additional objects, advantages and novel features of this invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by the practice of this invention. The objects and advantages of this invention may be realized and attained by means of the instruments and combinations particularly pointed out in the appended claims.

These and other objects of the invention are achieved by an electronics system, which in its present preferred embodiment employs an innovative Differential Frequency Shift Key (DFSK) modulation technique to improve the reliability and achievable data rates of Local Area Network (LAN) communication between digital computer workstations across Power Lines or Power Line Carrier (PLC) mediums. While the preferred embodiment of the system is designed to operate at data rates of up to 2 million bits per second (2Mbps), even higher data rates are possible with some envisioned enhancements, and very high noise, jitter, temperature, and voltage drift immunity.

Brief Description of the Drawings

Figure 1 is a diagram of a PLC LAN repeater network.

Figure 2 is a block diagram of a PLC LAN repeater.

Figure 3 is a schematic of a LAN to Repeater Interface.

Figure 4 is a schematic of a PLC Repeater Transceiver.

Figure 5 is a schematic of a standard quadrature detector for the demodulation of FSK carrier signals.

Figure 6 is an illustration of the voltage output from the quadrature detector buffer amplifier 5-54 (V_{quad}5-59), showing the variance of the voltage level with frequency change.

Figure 7a shows the schematic of a DC-coupled FSK data comparator. Figure 7b shows the ideal operation of the DC-coupled FSK data comparator. Figure 7c shows the operation of the DC-coupled FSK data comparator when there is signal drift.

Figures 8a, 8b, and 8c illustrate the operation and disadvantages of the traditional FSK data slicer 8-70.

Figure 9a illustrates the DFSK data detector of the preferred embodiment of the invention which overcomes the limitations of prior detectors. Figure 9b shows the nature of DFSK V_{quad} signals as they are detected by a quadrature detector. Figure 9c shows the effect of temperature or data composition on the operation of the DFSK data detector. Figure 9d depicts a further modification/enhancement of the DFSK demodulator.

Figure 10 illustrates a comparison of the frequency spectrum of FSK with DFSK modulation and illustrates the improved bandwidth requirements of DFSK over FSK.

Figure 11 illustrates the implementation of DFSK modulation using a 5-state digital state machine.

Figure 12 illustrates a state machine improvement where the data rate is synchronized with the carrier frequency.

Figure 13 is a MC13158 receiver data book chart for the RSSI response which shows a limiting characteristic RSSI detection schemes and protocols based on RSSI signals.

Figure 14 illustrates several improvements achieved with the Acknowledge Comparator.

Figure 15 depicts a typical $V_{quad,}$ data and FSK ACK Data waveform which illustrates how DFSK permits the compatible use of FSK to produce special characters for group acknowledgment in a network.

Detailed Description of the Preferred Embodiment

A universal local area network (LAN) power line carrier (PLC) repeater system and method is described which provides: (1) a competent LAN repeater interface for converting high-speed LAN data to PLC serial data and high-speed PLC serial data to LAN data, (2) a high-speed PLC data transceiver for exchanging PLC data with other repeaters, and (3) a control system and method for controlling the interface and transceiver to arbitrate data communications on the PLC bus among the plurality of PLC repeaters. In the following description, the Ethernet LAN PLC repeater is set forth in specific detail in order to provide a thorough understanding of the invention in a non-trivial application. It will be apparent to one of ordinary skill in the art that these specific details are beyond what is necessary to practice the present invention. In other instances, well-known circuits, interfaces and software structures have not been shown in detail in order not to unnecessarily obscure the present invention.

Reference is first made to Figure 1 in which a plurality of workstations are networked together by means of PLC repeater s and the AC power system of a premises. Workstation 1-1 with its corresponding LAN card is connected via UTP 1-2 to LAN-PLC repeater 1-3 to the AC power line 1-4 of a premises which constitutes a PLC LAN bus in addition to distributing AC power to the various appliances, equipment and workstations (1-1, 1-7, 1-10) of the premises. Data from workstation 1-1 is repeated onto the PLC LAN bus 1-4 in proper format for LAN-PLC repeater 1-5 to receive said data and repeat it in LAN format via UTP 1-6 to workstation 1-7 and its corresponding LAN card. Workstations 1-1, 1-7 and 1-10 are operated by commercial LAN software which, at a minimum, supports a peer-to-peer configuration of users, thus permitting messages and files to be transferred between any two peers of the network. The LAN PLC repeater permits said data to be transferred between workstations "transparently," that is, without any additional effort or special instructions/software on the part of the workstation and its operating system. Therefore, workstation 1-7 receives the data originating from workstation 1-1 and confirms receipt thereof back to 1-1 via UTP 1-6, repeaters 1-5, AC power bus 1-4, repeater 1-3 and UTP 1-2.

While two workstations networked together peer-to-peer constitute the minimum configuration of a network and do not require sophisticated network arbitration, many commercial network products assume that additional workstations, represented by 1-10, may be connected to the network, seeking network access simultaneous with other workstations and requiring CSMA/CD. In a PLC LAN repeater, arbitration protocols peculiar to the PLC environment need to be serviced transparently to the workstations/users.

Figure 1 also illustrates a segmented bus configuration comprising both a conventional hard-wired LAN bus segment 1-12 network and a PLC LAN interface 1-11. In this example, the LAN bus 1-12 networks physically proximate workstations together (not illustrated), while the PLC bus segment 1-4 could network physically less proximate or more mobile workstations 1-1, 1-7 and 1-10 to the network via PLC-LAN interface 1-11. Interface 1-11 is also a "repeater" similar in hardware to repeater 1-3, but may include software/firmware which identifies and repeats only those LAN packets/data addressed to workstations 1-1, 1-7 and 1-10 on the PLC LAN segment 1-4, thereby reducing the data traffic load on said PLC segment 1-4. In large networks involving many workstations, a plurality of PLC LAN segments 1-4, each operating on its exclusive PLC frequency and serviced by its respective PLC-LAN interface 1-11, may be networked together by means of the instant invention, while sharing the AC power distribution bus through frequency domain multiple access or other multiple techniques such as code division multiple access.

Referring still to Figure 1, other communication devices besides workstations may be represented by workstations 1-1, 1-7 and 1-10. For example, embedded microcontrollers 1-1 and 1-7 with communication ports could be networked through embedded repeaters 1-3 and 1-5 with a host controller 1-10 which monitors/controls the operation of the equipment hosting said microcontrollers. A relatively simple network communication and arbitration protocol could be administered by said host repeater 1-8. Such protocols have been developed for applications such as utility meter reading and industrial control systems.

Figure 2 is a block diagram of a LAN PLC Repeater 1-3. The LAN connection 1-2 to repeater 1-3 is made at RJ-45 connector 2-1, which is operably connected via connections 2-2 and isolator 2-3 to the differential transmit and receive ports 2-4 of LAN interface IC 2-5. Network Interface Controller (NIC) 2-5 (data sheets may be found in National Semiconductor's Local Area Network Databook, incorporated by reference) is a generic, multiple-sourced part which is common to most sophisticated LAN networks and contains the hardware registers, connections and logic/firmware to transmit and receive high bit rate LAN signals with standardized preambles, packet sizing and CSMA/CD collision arbitration. A standard RAM (Random Access Memory) 2-6 sufficient size is operably connected to NIC 2-5 via memory address and data bus 2-7 to store incoming and outgoing data packets: (1) incoming packets which have been received from LAN connection 1-2 and are waiting to be transmitted further by μC 2-9 and (2) outgoing packets which were received by μC 2-9 and are waiting to be transmitted back through LAN connection 2-1 to the network 1-2 or LAN card of a workstation 1-1. The repeater is controlled by μC 2-9, which is operably connected to NIC 2-5 via control, data and address lines 2-8, permitting the μC 2-9 to setup and control the NIC 2-5 and transfer data packets bidirectionally into/out of the packet buffer 2-6. In addition, μC 2-9 has communication ports, both parallel and serial, for communicating LAN data with wired and/or PLC interfaces. Some

commercial μC's, such as the Intel 83C152 (an 8031 derivative, data sheets for which may be found in Intel's Bit Embedded Microcontroller Handbook, incorporated by reference) contain high-speed Global Serial Channels (GSC) 2-10 which are capable of 0.1 – 10 Mbps serial data transfer with CDMA/CD protocol registers and firmware at a reasonable cost, which facilitates data I/O for a high-speed PLC transceiver (2-11 through 2-17 or Figure 4), which is operably connected to the global series channel 2-10. Transmit data TXD from the incoming packet buffer 2-6 modulates an RF carrier at modulator 2-11 which drives transmitter 2-12, which transmitter is operably connected to the power line bus 1-4 via Filter 2-13 and RF coupler 2-14. Transmitter 2-12 is turned ON by transmit enable TXE only when data is transmitted, thus reducing the RF traffic on the AC line 1-4 during latent periods. Data receiver 2-16 is operably connected to AC bus 1-4 via RF coupler 2-14 and filter 2-15. Data-modulated RF from similar repeaters carried by power line 1-4 is received by the receiver 2-16, buffer by high-speed comparator 2-17 and transferred as RXD to global serial port receiver 2-10where μC 2-9 screens the preamble for ID codes/addresses and arbitrates the data for transmission on to the LAN interface. Unique ID codes repeater addresses may be either manually entered by dipswitch or automatically assigned by network supervisory software under automatic or user control. For example, manual entry ID code switches 2-22 operably connect to a port of the μC 2-9 via lines 2-21, and may be used to uniquely identify address and security bytes in preambles and/or determine arbitration backoff delay times, etc. Factory-burned ID codes can also be obtained with specialty or ASIC designs.

Figure 2 also illustrates alternate LAN and data sources for the PLC repeater. The μC 2-9 provides a standard serial comm port 2-20 which connects to a serial port interface 2-19 and connector 2-18, configuring repeater 1-3 into an RS-232D LAN repeater, in which the PLC data transceiver operates at substantially higher data rates (than the 115.2Kbaud RS-232D) to unburden the AC power bus 1-4 LAN. (The Network Interface Controller and associated parts would be removed, if unused in this alternate embodiment.) IN some network configurations, parallel port interface components could be operably connected in place of serial components 2-18 and 2-19 to a parallel port on μC2-9. Alternately, the GSC port 2-10 could be operably connected to an RS-485 LAN via a 2-19 interface like the LTC490, while the μC serial port 2-20 TxD and RxD lines could be operably connected to the TXD and RXD I/O 2-11 and 2-17 of the PLC transceiver. In its simplest embodiment, the TxD and RxD lines 2-20 may be operably connected to TXD and RXD lines 2-10, providing a repeater requiring μC; PLC transmitter 2-12 and receiver 2-16 have been operated simultaneously on different carrier frequencies to provide full duplex serial operation, if required by the LAN application. Alternately, the transmitter in a no μC system may be enabled only when data is transmitted, to permit PLC LAN operation with a single frequency.

Figure 3 presents a detailed working schematic of the LAN interface and 10 Mbps to 1 Mbps converter. J1 2-1 is the RJ-45 connector to the LAN line/card of a workstation. U3 2-3 is the Isolator/Filter for Ethernet 10Mbps lines. U1 2-5 is the NIC chip, a National DP83902A, the complete specs for which are found in National Semiconductor's Local Area Network Databook, already incorporated by reference, which also contains comprehensive documentation on the Ethernet IEEE 802.3 standard. Several Network Interface Controllers are available from various manufacturers for Ethernet as well as other popular network standards, such as Arcnet and Token Ring, which may be operably connected to μC U6 2-9 in place of Ethernet NIC 2-5 and the corresponding connectors 2-1 through 2-4.

Referring still to Figure 3, an 8Kbyte RAM packet buffer U5 2-6 is operably connected via address latch U7 3-27 to the memory address and data ports of NIC 2-5. The size of buffer 2-6 may be enlarged or reduced somewhat to accommodate network data capacity, system operation and budgetary constraints. Repeater μC U6 2-9 is operably interfaced with NIC U1 2-5 via latches, U13, U14 3-25 & 3-26 and PAL U15 3-28. The timing diagrams and PAL 3-28 logic diagram are appended herewith in Appendix B. Additional functions 20 MHz clock 3-29, 10 MHz divider 3-30, status drivers 3-31 and status indicators D1, D2 and D3. While one enabling embodiment has been represented, those skilled in the art will appreciate that other approaches and simplifications can be implemented without departing from the method presented herein.

Referring to Figure 3 again, the μC 2-9 may contain masked ROM firmware or may be operably connected with external EPROM U9 3-9 for development purposes. A pseudo-code listing follows:

LAN PLC REPEATER PSEDUO-CODE FLOW SHEET

```
RESET ON POWER UP
STARTUP SEQUENCE
'Initialize μC sets up the communications registers for Manchester
'Encoding with CSMA/CD. A 16-bit CRC is selected and the preamble
'is set to 8 bits. The serial rate is set to 1.25Mbps.
INITIAZLIE μC
        GMOD Register
                Select Manchester Encoding
                Select CSMA/CD
                Enable CRC, Select 16-bit CRC
                Set preamble to 8 bits
        Baud Register
                Set serial rate at 1.25 Mbps
        Disable all interrupts
        Enable receiver
        Set transmit status register to normal operation
        Set address mask registers to don't care state
        Initialize SLOTTM (slot time register) to 2μs
'Initialize NIC divides the 8K buffer into 2 Xmit buffers and 20
'256 byte pages for the receive ring. Data is handled a byte at 'time and the FIFO to receive buffer ring occurs 8
bytes at a time.
'The CRC is appended by the transmitter. The receiver rejects 'errored packets. All valid packets are received.
INITIALIZE NIC
        Setup 8K xmit/rcvr buffer
        Setup 2 Xmit buffers of 1536 bytes each
```

```
    Set remaining 5120 bytes as receive buffer ring
    SETUP NIC REGISTERS:
        Data Configuration Register
            Byte wide DMA transfer
            Normal operation
            FIFO set to 8 bytes
        Transmit Configuration Register
            CRC appended by transmitter
            Normal operation
            Normal backoff
        Receive Configuration Register
            Reject packets with receive errors
            Reject packets with fewer than 64 bytes
            Accept broadcast packets
            Accept all packets (promiscuous mode)
            Buffer packets to memory
'The µC Receive Routine keeps track of the current NIC transmit
'buffer then loads that buffer data as it is received in the
'µC Receive FIFO.
RECEIVE Routine: (µC ROUTINE for µC to send data to NIC)
    Choose free NIC transmit buffer
    IF NIC transmit buffers full, THEN
        Discard receiver and GOTO TRANSMIT
    Check Receive FIFO for Not Empty (NE) flag on µC
    Read byte from Receive FIFO
    Check Receive FIFO NE flag on µC
    IF FIFO Empty, THEN validate byte (No collision packet byte)
        IF transmit pending, THEN
            Restart backoff
        ELSE GOTO RECEIVE ROUTINE:
    ELSE GOTO READ ROUTINE (Valid Data Packet)

    READ ROUTINE: Write byte to NIC transmit buffer
        Read FIFO NE flag
        IF NE flag asserted, THEN GOTO READ ROUTINE
        ELSE write last data byte to NIC transmit RAM
```

```
                (Packet has been read and written to NIC)
            Check receiver for receiver errors
            IF no errors, THEN
                Instruct NIC to transmit Packet
            ELSE discard packet
            GOTO TRANSMIT
'The µC Transmit Routine checks its Global Serial Channel (GSC) for
'a not busy state.  If the GSC is not busy then the µC reads packet
'data from the NIC and loads the TX FIFO.
TRANSMIT ROUTINE:  (routine for µC to get data from NIC)
        IF NIC has received a valid packet, THEN
            IF Global Serial Channel (GSC) is not busy, THEN
                Get pointer to received packet
                Read 2 bytes from NIC
                Save 1st byte (this is a pointer to the next received packet)
                Read 2 bytes from NIC
                Save these bytes in variable ByteCount

                LOOP
                    Wait TX FIFO Not Full (NF Flag)
                    Read 1 byte from NIC
                    Write 1 byte to µC TX FIFO
                    Decrement ByteCount
                ENDLOOP (When ByteCount is zero)
        ELSE GOTO RECEIVE ROUTINE
```

An additional routine services AC PLC bus collision avoidance and access arbitration. The method requires each repeater (with data to send) seeking access to a particular frequency or channel of the AC LAN bus (1) to listen to the bus traffic and, upon detecting the termination of a third party transmission, (2) to wait a minimum of 20 μs plus a random additional time (in 5 μs increments) before transmitting a short access request. (3) Following the access request, the receiver listens for 15 μs and, upon detecting no other carrier, the repeater μC begins data transmission with confidence. The dipswitch 2-22 may be used to provide a unique backoff or wait time for each repeater in addition to providing a unique IC code/address.

The universal interface capabilities of the controller 2-9 with its parallel and serial ports provides the capability for embedding the PLC repeater in computers and equipment with embedded controllers which already

connect to the AC power system of a premises, thereby networking the equipment with other similarly equipped devices and users simply by connecting the AC power. The physical size of such system and its associated cost could be reduced by utilizing the existing embedded controller and its serial port as the repeater controller and merely interfacing it to a compatible embedded PLC transceiver. The embedded controller would require the addition of appropriate network arbitration and control software/firmware. State-of-the-art design and manufacturing techniques reduce size and cost of repeater systems to attractive marketing levels.

Referring now to Figure 4, a versatile PLC data transmitter and receiver are shown which provide DC to 2 Mbps data rates. No Manchester or other encoding is required. Wideband data or analog signals may be transferred in original form. The data interface of the transceiver comprise four data lines: a transmit data input line GTXD, a transmitter enable input line TXE, a receive data output line GRXD and a carrier detect output line CARDET. These lines correspond to their counterparts at the Global Serial Channel 2-10 of the μC 2-9. GTXD data voltage levels are coupled to varactor diode D7, which is capacitively coupled to the frequency determining components C18 and C22 at the low-impedance port of oscillator 2-11, of which transistor Q3 4-33 forms the active element. Changes in reverse voltage across D7 result in corresponding inverse changes in the junction capacitance of D7 which change the resonant frequency of oscillation determined by L3 and the combination of C18 with the other capacitors C19 through C24. Driving the low-impedance port of oscillator 2-11 at the collector of Q3 4-33 minimizes the negative impact of differentiated DC voltage shifts on the delicate bias of Q3 4-33, which DC sifts correspond to differentiated data coupled through capacitors C19 and C22. The output of Q3 drives a class D output stage 2-12, which efficiently drives the power line through filter 2-13 and RF coupler 2-14. The several stages of transmitter drivers buffer the oscillator 2-11 from AC line capacitance and load changes. A class A transmitter output may be employed to reduce harmonics but with decreased efficiency. The transmitter enable TXE circuit 4-34 connects to the base of Q3 4-33 through D6 to turn the oscillator 2-11 off. The circuit of 4-34 may be configured as an inverter (for operation from a controller) or as a resetable monostable multivibrator (for enabling the transmitter only when data is presented to the data input).

Figure 4 also shows a data receiver 2-16 which is coupled by 2-14 RF coupler and filter 2-15 to the AC power bus. The filter 2-15 selects only the desired frequencies and matches the impedance of the AC line to that of the receiver input pin 1. The receiver 2-16 is a high performance superhetrodyne design with local oscillator, mixer, 2 stages of IF gain/filtering and limiter with quadrature detector, providing over 90 dB of RF gain with DC to 2 Mbps data response (Philips SA 636 version). The receiver 2-16 local oscillator supports either (1) crystals, (2) LC oscillators or (3) external oscillator/synthesizers. Use of a synthesizer permits controller 2-9 selection of LO frequencies for FDMA and frequency hopping configurations. Receiver 2-16 has both a data output and a competent FSI (Field Strength Indicator) output, which are buffered by high speed comparators 4-35 and 4-36 such as LM319 or LM360. It should be noted that an analog buffer can be connected to the demodulated signal output (pin9) of the receiver 2-16 for recovery of Wideband analog or composite analog/digital signals. The FSI CARDET output supports the RF carrier detect input of the repeater controller 2-9 for performing AC bus arbitration. The CARDET and GRXD buffered comparator outputs may be connected together in a wired AND configuration to provide

data output only when BOTH the carrier is present AND data is present. The receiver 2-16 is so selective that multiple receivers and transmitters may be used simultaneously in a repeater to increase data rate, increase channels or network together AC power line LAN segments. The transmitter and receiver are fully capable of RF LAN operation which, in conjunction with the competent collision avoidance and arbitration, would provide competent RF LAN segments for many applications.

It should be noted that alternative commercial components of competent specifications can be used for the components specified herein. Although this invention has been illustrated in relation to a particular embodiment, it should not be considered so limited except by the appended claims.

Alternative embodiments of the PLC transceiver hardware can provide significant improvements in data rate while increasing system reliability. These alternatives employ a different modulation technique than the FSK described previously, where detection was done by analog comparator DC threshold adjustments in reference to an analog demodulated FSK data waveform. This previously described FSK modulation technique produced a waveform which at high data rate exhibits a ramping/semi-sinusoidal characteristic (instead of the ideal DC square waves produced at low data rates). The alternative embodiment, described following, uses a Differential Frequency Shift Key (DFSK) in conjunction with the FSK modulation technique. DFSK produces sharp data edges for triggering the data detector and further permits AC coupling of said data edges, improved speed of data demodulation, and increased data reliability – less subject to system temperature coefficients, while minimizing the required effective bandwidth for a given data rate by centering more energy around the carrier frequency.

Further improvements are incorporated in this alternative transceiver embodiment, including: improvements in RF and IF filters to provide wider and flatter pass bands while maintaining reliability with changing data compositions, an introduction of a realignment bit in the data to provide the means for allowing the receiver to re-synchronizing with each in-coming byte, improvements in carrier detection and acknowledgment, and an improved controller.

These improvements permit a dramatic improvement in data rate and bit error rate across the PLC interface, from previous speeds of 100 to 350 Kbps to 1-3 Mbps. The following discussion describes prior modulation circuits, their characteristics and the current best mode of the invention utilizing the DFSK modulation techniques.

Figure 5 illustrates a standard quadrature detector for demodulation of FSK carrier signals. The IF limited output 5-51 of a receiver IF section (for example as shown on Figure 4 at U1 2-16 pin 11) drives directly the first input 5-56 of a quadrature detector 5-50 (which is typically an analog Gilbert cell multiplier). Said IF limiter also drives loosely, through a small-valued, high-impedance capacitor C1 5-55, a quadrature tank circuit composed of an inductor L 5-56, an capacitor C 5-57 and a resistor R 5-58. The capacitor C1 5-55 is typically a small value, such as 5pF in order to avoid swamping the transfer function of the quadrature tank circuit. The typical values of L 5-56, C 5-57 and R 5-58 depend on the carrier frequency. For example: for a 10.7 MHz system L 5-56 would typically be 1.5μH, C 5-57 would typically be 139pF, and R 5-58 would typically be 2.2KΩ; while for a 20 MHz system L 5-56 would typically be 1.5μH, C 5-57 would typically be 39pF and R 5-58 would typically be 4.7kΩ. The

quadrature tank circuit drives the second input 5-52 of the quadrature detector 5-50. The quadrature detector 5-50 is a multiplier which produces an output voltage QuadOut 5-53 that is the product of the two sine wave input signals. The double frequency output component of QuadOut 5-53 is filtered and amplified by the detector buffer amplifier 5-54, leaving the phase differential component V_{QUAD} 5-59 which varies in magnitude according to the frequency difference between the IF frequency received from a transmitter 5-51 and the quadrature tank resonant frequency determined by L 5-56 and C 5-57, as described in Figure 6. V_{REF} 5-66 is maintained at a voltage between the V_{QUAD} 5-59 FSK 1 and 0 levels, by the diodes D1 5-61 and D2 5-62 Comparator/Data Slicer 5-60 outputs data 5-64 at logic levels to a deserializer. The quality of the Data Slicer 5-60 is determined by how well it defines or recovers from V_{QUAD} 5-59 the edges of each data bit. Indeed, the quality of a complete modulation and demodulation system is determined by how faithfully data is transferred from the data transmitter to the data receiver. Prior data slicers exhibit two significant problems that are overcome by the present invention: (1) sensitivity to voltage drifts in V_{QUAD} 5-59, and (2) sensitivity to high data rates and data composition, as illustrated in the discussion and figures that follow.

Figure 6 illustrates that V_{QUAD} 5-59, the output of the quadrature detector buffer amplifier 5-54, varies lineraly with IF frequency within a 400KHz range. The attractive feature of this type of demodulator is that V_{QUAD} 5-59 is a DC level signal directly related to frequency, i.e., a 200KHz IF signal f_0 produces a +400 mV V_{QUAD} 5-59 signal and a +200 Khz IF signal f_1 produces a –400 mV V_{QUAD} 5-59 for low to intermediate data rates. The comparator 5-60 reference voltage V_{REF} 5-66 is maintained at a voltage corresponding to the virtual center frequency f_c between f_1 and f_0. Figure 6 also shows V_{QUAD} drift as a DC offset to the quadrature detector transfer characteristic at f_c about V_{REF}. V_{QUAD} drift is caused by the sum of temperature coefficient and long term frequency drifts of the transmitter and the receiver local oscillator in addition to the temperature coefficient and mechanical vibration drifts of the quadrature coil L 5-56 and capacitor C 5-57. The temperature coefficient drifts of quadrature detector 5-50, buffer 5-54 and comparator 5-60 are minor because V_{QUAD} is in the 400 mV range.

The prior DC coupled data slicer illustrated in Figure 7a may be less sensitive to data composition but is likely to be very sensitive to V_{QUAD} drifts. A second prior data slicer circuit, shown in Figure 8a, can track temperature coefficient and drift changes for low data rates, but no for high data rates or mixed data compositions.

At higher data rates, the V_{QUAD} buffer 5-54 slew rate combined with the time domain response limitations due to the bandwidth of the IF filters produce lower amplitude V_{QUAD} output signals are shown in Figure 7b. A lower data rate 3-bit long (0 0 0) V_{QUAD} signal is compared to a higher data rate single bit V_{QUAD} signal (0 1 0). While t1 through t3 is the period of a single high data rate bit, t1 through t7 is the period of a 3-bit long V_{QUAD} signal. At the higher data rate, the peak amplitude of V_{QUAD} at t2 and t4 is significantly lower than for the 3-bit long V_{QUAD} signal peak at t4 (and t10). The variation in V_{QUAD} peak voltage with data composition is significant enough to foil the operation of the V_{REF} bias circuit of Figure 5, but not that of Figure 7a, which illustrates a prior DC coupled data comparator with fixed reference (V_{REF}) as set by resistors R1 7-67 and R2 7-66. R1 7-67 and R2 7-66 are typically set to 1 kΩ. But while the DC coupled comparator of Figure 7a is able to slice the data from higher data rate or mixed data composition V_{QUAD} 7-68 signals illustrated in Figure 7b, it yet experiences significant data edge and bit

width symmetry difficulties when encountering temperature coefficient and signal drifts. Figure 7c illustrates the negative effects of V_{QUAD} 7-68 drift on the data 7-69 signal. The width of the 0 bit is totally truncated form t1 to t3, while the width of the 1 bit is expanded accordingly.

Figures 8a through 8c illustrate the operation and disadvantages of the FSK data slicer 8-70 with tracking reference V_{REF} 8-71 provided by diodes D1 8-73 and D2 8-74 and hold capacitor C_{hold} 8-75. D1 8-73 and D2 8-74 become forward biased during the positive and negative peaks of the FSK V_{QUAD} 8-72 signal and ensure that C_{hold} 8-75 is charged to the peak FSK V_{QUAD} voltage value less the diode forward voltage drop (about 40 mV). Thus, if the gain of buffer 5-54 is adjusted to provide an 800 mV peak-to-peak V_{QUAD} signal to D1 8-73 and D2 8-74, C_{hold} 8-75 will be charged by D1 8-73 and D2 8-74 after a few lower data rate alternating bit cycles to an intermediate value of V_{REF} halfway between the 0-rail and 1-rail of V_{QUAD} 8-72 that ideally provides adequate comparator 8-70 "slicing" of data from V_{QUAD} 8-72, as illustrated in Figure 8b. However, as illustrated in Figure 8c, when lower amplitude high data rate signals are used (for which the peak amplitude of V_{QUAD} 8-72 is reduced below the forward voltage drop of D1 8-73 and D2 8-74) or when long strings of 1's or 0's present in the data, the slicer V_{REF} 8-71 begins to drift off of the ideal center voltage and causes corresponding data edge and width distortions as shown in Figure 8c. The width of high data rate bits at t2-t9 are significantly distorted. And while the string of 1's at t9 to t13 may have readjusted V_{REF} for a time, at t12 other drift factors such as diode D2 8-74 leakage or comparator 8-70 input bias currents have started changing the charge on C_{hold} 8-75 with the attendant drift of V_{REF} 8-71/

Figure 9a illustrates a DFSK data detector 9-77 which overcomes the limitations of prior detectors. Both comparator inputs 9-78 and 9-79 are DC biased identically by means of R1 9-80 and R2 9-81 through R3 9-82 and R4 9-83 to V_{REF} 9-88 and the V_{QUAD} 9-84 DFSK signal illustrated in Figure 9b is AC coupled to the inverting comparator 9-85 input (V_{QUAD} 9-78) through capacitor C3 9-86. C2 9-87 bypasses or filters V_{REF} 9-88 from the AC signals at both inputs 9-78 and 9-79 of the comparator 9-85 passed to V_{REF} 9-88 through R3 9-82 and R4 9-83. R3 9-82 (from the DFSK V_{QUAD} 9-78 signal) and through R4 9-83 (from the V_{+REF} 9-79 noninverting input of comparator 9-85).

Figure 9b illustrates the nature of DFSK V_{QUAD} signals as they are detected by a quadrature detector. Differential frequency signals may be characterized by a short decrease in frequency to represent a falling edge (or high to low logic level change) in data. The term "differential frequency shift key" arises because the DFSK V_{QUAD} data looks like the derivative or differential of the FSK data described in Figures 6, 7 and 8. A DFSK modulation technique will be described in Figure 11. Figure 9b represents the signals at the inverting input (V_{-QUAD} 9-78), noninverting input V_{+REF} 9-79 (the dashed lined) and data output of data slicer comparator 9-85 of Figure 9a. The inverting input signals V_{QUAD} 9-78 comprise a DC component equal to V_{REF} 9-88 and an AC component equal to V_{QUAD}'s DFSK component. Thus, at t0 the carrier frequency is f_0, V_{QUAD} 9-84 is at its median level, and V_{QUAD} 9-78 is at V_{REF} 9-88, its DC level provided by R3 9-82. AT t1 to t4 a DFSK falling data edge signal is detected as a positive pulse at V_{QUAD} 9084 and transferred through C3 9-86 to V_{QUAD} 9-78. Meanwhile, at t0 V_{REF} 9-79 is more positive than V_{REF} 9-88 due to the voltage divider action of hysteresis resistor R_H 9-89 with R4 9-83 and the logic level 1 data output voltage of the comparator 9-85. R_H 9-89 and R4 9-89 and R4 9-83 are judiciously selected to provide sufficient

hysteresis to permit noise reduction of half the V_{QUAD} 9-84 peak signal level or 200 mV (since the peak value of V_{QUAD} 9-78 is about 400 mV). Therefore, when the V_{-QUAD} 9-78 signal rises at t2 to V_{+REF0}, comparator 9-85 output state toggles to logic 0 with a corresponding change in V_{+REF} 9-79 to V_{+REF1}. At t4 V_{-QUAD} 9-78 returns V_{REF} 9-88 until t5, when a negative going V_{QUAD} 9-78 voltage (1 level data edge) DFSK transition starts. At t6 V_{QUAD} 9-78 drops to the V_{+REF1} voltage, the comparator 9-85 data output again toggles from 0 to 1 logic level with a corresponding to a change in V_{+REF} 9-79 to V_{+REF0}, where the reference input of the comparator waits until the next 0 level t1 to t4 type V_{-QUAD} 9-78 signal is detected.

Because the DFSK signal defines the edges of each data level change, there is no temperature drift or data composition component that foils the operation of the comparator 9-85 DATA output 9-90, as illustrated in Figure 9c. The time constant of C3 9-86 and R3 9-82 is selected to be long enough to pass DFSK V_{QUAD} to the inverting input of comparator 9-85 (V_{-QUAD} 9-78) but short enough to reject short term DC drifts present V_{QUAD} 9-84 due to data composition changes and to adjust quickly to the transient DC change from noise to preamble exhibited upon initial receipt of a packet. The time-constant value (τ=R3 9-82 x C3 9-86) can be about 5 μs for data rats in the megabit range. Hysteresis in the comparator circuit (provided by R_H 9-89 and R4 9-83) provides the same noise rejection characteristics as ordinary FSK and in the instant circuit may be 400 mV total for an 800 mV peak-to-peak V_{QUAD} 9-84 signal. (input offset drifts in comparators are typically below the millivolt level, while signal levels are hundreds of millivolts.) Typically, in the current best mode of the invention C3 9-86 is 470 pF; C2 9-97 is .1 μF; R1 9-80 is 1 kΩ; R2 9-87 is 1 kΩ; R3 9-82 is 10 kΩ; R4 9-83 is 33 kΩ; and R_H 9-89 is 470 Ω.

A further modification to the DFSK demodulation scheme provides for peak detection of the demodulated data pulses, since the time location of DFSK peaks tend to be more stable with variation in real media amplitude and phase attenuation characteristics. A peak detector is illustrated in Figure 9d. The peak detector consists of two sets of analog voltage comparators 9-91, 9-92, 9-93 and 9-94, one set of which (9-93 and 9-94) detects the level of the peaks of the demodulated data signal (through C3 9-95 and R3 9-96) and another set of which (9-91 and 9-92) detects the zero-slope of the peaks by differentiating the demodulated signal (through C5 9097 and R5 9-98). The time constant of C3 9-95 and R3 9-96 is selected to be longer than the data time constant (τ = 470 pF x 10 kΩ - 4.7 μs), while the time constant of C5 9-97 and R5 9-98 (τ = 68 pF x 1 kΩ = 68 ns) is selected to be short with respect to the raw data waveform V_{QUAD} Bias and reference levels for the comparators are provided by R1 9-99, R2 9-100, R6 9-101, R7 9-102, R8 9-103, and R9 9-104 providing the upper and lower peak detection reference voltages DU 9-105 and DL 9-106 for AC-coupled data VD, permitting peak detection to be performed by comparators 9-93 and 9-94. R6 9-101 and R7 9-102 provide ZU 9-107 and ZL 9-108, the upper and lower references for zero slope detection by comparators 9-91 and 9-92. The open collector outputs of the comparators require pull-up resistors (R11 9-109, R12 9-110, and R13 9-111) and may be connected in a wired-NOR configuration, which for comparators 9-91 and 9-92 provides a 1 output for zero-slope signals. The peak and zero-slope outputs are then logically ANDed by NAND gates 9-112 and 9-113 to provide trigger pulses corresponding to the positive and negative peaks of the demodulated data signal. The positive peak pulse triggers the "0" state of the RS flip flop comprising gates 9-114 and 9-115 while the negative peak pulse triggers the "1" state of said RS

flip flop. In the current best mode of the invention the components have the following values: C5 9-97 is 68 pF; C2 9-116 is .1 μF; C3 9-95 is 470 pF; R1 9-99 is 1 kΩ; R2 9-100 is 1 kΩ; R3 9-96 is 10kΩ; R5 9-98 is 1kΩ; R6 9-101 is 8.2Ω; R8 9-103 is 75Ω' R9 9-104 is 75Ω; R11 9-109 is 470Ω; R12 9-110 is 1kΩ; and R13 is 1kΩ. It should be noted that digital signal processing hardware and firmware can provide many of the demodulation and data detection functions described herein, but at the higher cost of DSP chips and A/D converter interfaces.

Figure 10 compares the frequency spectrum of FSK and DFSK modulation and illustrates the beneficial bandwidth consumption characteristic of DFSK over FSK. AT low data rates (Figure 10a) FSK is designed to produce a fixed shift or deviation determined by the two frequencies assigned to the '1' and '0' data bits, the deviation (difference) of which is determined by the demodulator transfer function or curve (illustrated in Figure 10 as f_0 and f_1). The power of the FSK transmission is divided equally (for data with equal averages of 1's and 0's) between the two frequencies. At high data rates (Figure 10b) FSK exhibits sidebands spaced from the center f_c. At high data rates (Figure 10d) DFSK exhibits sidebands of the same width as with FSK, but the magnitude of the sidebands is suppressed by as much as 10dB compared to FSK, requiring less filtering of transmitter sidebands and better propagation through receiver filters.

DFSK modulation of a carrier is easily implemented with a 5-state digital state machine (driven by a 4 x f_c clock) as illustrated in Figure 11a, because (1) only one carrier/clock frequency need be generated or synthesized (as opposed to two with FSK) and (2) the rising and falling edges of the data are used to skip or add a state to the state machine, producing a higher or lower differential frequency shift, respectively. In the case of the normal unmodulated carrier f_c (with 50/50 duty cycle), the state sequence for one carrier cycle is 1,2,3,4 with states 1 and 2 producing a high level and 3 and 4 producing a low level. A falling data edge '0' causes the state machine to add a fifth state 2' between states 2 and 3, producing the sequence of 1,2,2',3,4 and resulting in a lower differential frequency shift corresponding to falling edge '0'. Similarly, a rising data edge '1' causes the state machine to skip state 2, producing the sequence 1,3,4 and resulting in a higher differential frequency shift corresponding to rising edge '1'. Thus, the DFSK state machine and modulation technique effectively has 3 symbols: (1) the rising edge of data, (2) the falling edge of data, and (3) no data edges or state changes, which further distinguishes DFSK from other modulation techniques (FSK, QFSK, PSK, QPSK, etc.) that have 2 or 4 or more (even numbers) symbols, but not 3. It should be noted here that the 5-state digital state machine in practice employs more states to permit setup, synchronization and timing of data with carrier. Also, the assignment of data logic states to higher or lower differential frequency shifts may be reversed from the example herein without changing the substance of the invention.

Additional state machine modifications illustrated in Figure 11b permit selection of alternate data rates while keeping carrier frequency fixed by selecting a preset number n of carrier cycles per bit. A presetable divide by n counter may be added to the state machine to provide a data clock which is presetable submultiple of carrier frequency. Thus, a 6 MHz carrier would provide bit rates corresponding to n as follows: 1200 kbps for n=5, 600 kbps for n=10, 300 kbps for n=20, and 150 kbps for n=40. Selection of bit rate without changing carrier frequency by system controllers permits negotiation of bit rate for servicing a variety of device types on a network

as well as accommodating varying power line propagation characteristics. For example, a lowest cost light switch node may be implemented with 150 kbps monolithic filters and no data rate negotiability, while a moderate price point printer node may be operated at 1200 kbps with discrete wideband filters and have negotiability designed into its controller. By initiating operation of the network at 150 kbps, the n for the printer and the switch would start at 40, but as soon as the device type and node address were broadcast for a printer node, the bit rate would be negotiated upward from n=40 to n=20 until n=5 or until the bit error rate became unacceptable for the conditions of the power line medium at that time, whereupon the n and corresponding data rate would back off to an acceptable selection.

An addition advantage of the DFSK modulator is that the state machine can be configured and instructed by a data controller to produce special DFSK characters for control or compression purposes. For example, two lower differential frequency shifts could be executed in sequence to represent a string of 1's while two higher differential frequency shifts in sequence could represent a string of 0's. This feature is not possible with FSK. The state machine has no limitations on its agility regarding which states it adds or skips, as instructed. The demodulator data slicer would require some additional comparator(s) and logic/circuitry to detect successive DFSK pulses of like polarity.

An additional modification to the carrier generation and modulation state machine includes increasing the number of states to permit Multiple DFSK techniques. For example, subdividing the original 5 states by 2 doubles the number of states to 10 half-states (with a corresponding doubling of clock frequency to 8 x f_c) and permits increasing the number of symbols by 2 by skipping or adding 1 or 2 half-states. Corresponding modifications to the receiver demodulator are required to detect the differing responses to the 1 and 2 half-state symbols. Since a 1 half-state shift produces half the differential frequency shift of a 2 half-state shift, a quadrature detector produces pulses of half the amplitude for the 1 half-state shift with reference to a 2 half-state shift, which is the normal shift for standard DFSK.

A further modification to the carrier generation and modulation state machine includes modulation shaping methods that more consistently define data edges at high bit rates, which modifications either prefix or append to data symbols (a) single whole shifts or (b) 1 or 2 half-state shifts which precompensate the quadrature detector's analog data output waveform for more accurate data slicing of each data bit sequence/combination.

DFSK, while discussed in this specification, primarily in a PLC application has many similar applications in other electronic communication system, including but not limited to: RF, wired, telephone line and the equivalent. Moreover, while this discussion of DFSK implies a workstation computer device, this technology can be applied, and should be considered within the scope of this patent, to any other electronic devices with communication capabilities, including but not limited to controllers, personal computers, fax machines, printers and telephonic systems.

Figure 12 illustrates the improvement in data bit timing accuracy achieved if the data rate is synchronized with the carrier frequency f_c and clock. Figure 12 shows two data bits of identical length or rate, XMIT DATA and XMIT DATA', but shifted in phase in reference to the CARRIER modulator. XMIT DATA falling edge X0 (and X0') and rising edge X1 meet the set up windows (low state) for the modulator state machine, while the rising edge X1'

of XMIT DATA misses the setup window of the modulator state machine, delaying execution of the modulation for rising edge 1 to 1', to the next CARRIER cycle and producing a corresponding time delay/shift in rising edge RCVR DATA R1 vs. R1'. Received data bit width changes of 1 carrier cycle produce significant data errors at the high data rates of the instant invention, while prior system data rates, being at least an order of magnitude lower, have not observed this error source as significant. It should be especially noted that both rising and falling edges of data are sensitive to data synchronization with the carrier modulator and that the variation in bit width data error is especially exacerbated by data rates that are not related to the carrier frequency by an even multiple of carrier cycles. Therefore, synchronization of both data rate and phase with the carrier modulator eliminates synchronization granularity/jitter in the modulated carrier, enabling high data rates.

Another improvement that increases the reliability of detecting/receiving the bits in each byte provides a realignment bit at the end of each byte. The realignment bit resynchronizes the receiver's deserializer sampling clock with each incoming data byte to prevent clock timing skews between the transmitter data clock and the deserializer (receiver) clock, permitting low-cost clock references. This differs significantly from other packet transmission schemes such as Ethernet, which employ 20,00000 MHZ (1ppm) accurate clocks for tracking a 1500-byte-long packet. While the realignment bit improvement is similar in concept to RS-232 start and stop bits, it differs significantly from RS-232 in that (1) the polarity alternates from that of the last data bit of the byte to further distinguish its edge from the last bit, and (2) only one realignment bit per byte is required, effectively reducing the overall data rate throughput by only 11% (as compared with 25% for RS-232). This improvement permits reliable data transfers at higher data rates well beyond the 11% hit as well as increasing the maximum packet size, while still permitting the use of low-cost clock references/crystals.

Figure 13 illustrates another limiting characteristic of prior techniques using RSSI detection schemes and protocols based on RSSI signals. Figure 13 shows an MC13158 receiver data book chart for the RSSI response. In networks involving RF carrier transmissions, each node has a transmitter and a receiver, the operation of which is determined by the fundamental protocol of the network (client-server, peer-to-peer, etc.). For data transmission, only one transmitter at a time is permitted to be active on the medium and then only when the respective node has data to send. When not transmitting, each node's receiver is active, producing valid data or spurious noise depending on whether a valid transmission is present on the medium. Prior network arbitration protocols have used the presence or absence of carrier as detected by receiver RSSI circuits to determine (1) that the data output of a receiver is valid or spurious, or (2) that the medium is clear of other transmissions, permitting a node's transmitter access to the medium. In each instance the response time of the RSSI circuit limits the responsiveness of system protocols as illustrated in Figure 13. The response time exceeds 4 μs for rise time t_r (presence of carrier) and exceeds 25 μs for fall time t_f (absence of carrier) for stronger signals, varying down to 6 μs for weak signals. Since the length of a byte at 2 Mbps is 4 μs, the six times variation between rise and fall times and the long length of the fall time (exceeding 6 data bytes) create bandwidth consuming protocol delays for send/receive and intergap spacing operations when the RSSI signal is used to arbitrate transmissions.

Then there are two other problems related to the nose level of the medium, and particularly that of the power line: (1) medium noise pulses trigger counterfeit RSSI signals and false arbitration attempts and (2) the signal-to-noise ratio on the medium changes from one environment to another and at different times of the day, making it difficult for an RSSI comparator circuit to adjust its reference to remain sensitive to normally attenuated signals while ignoring false triggers.

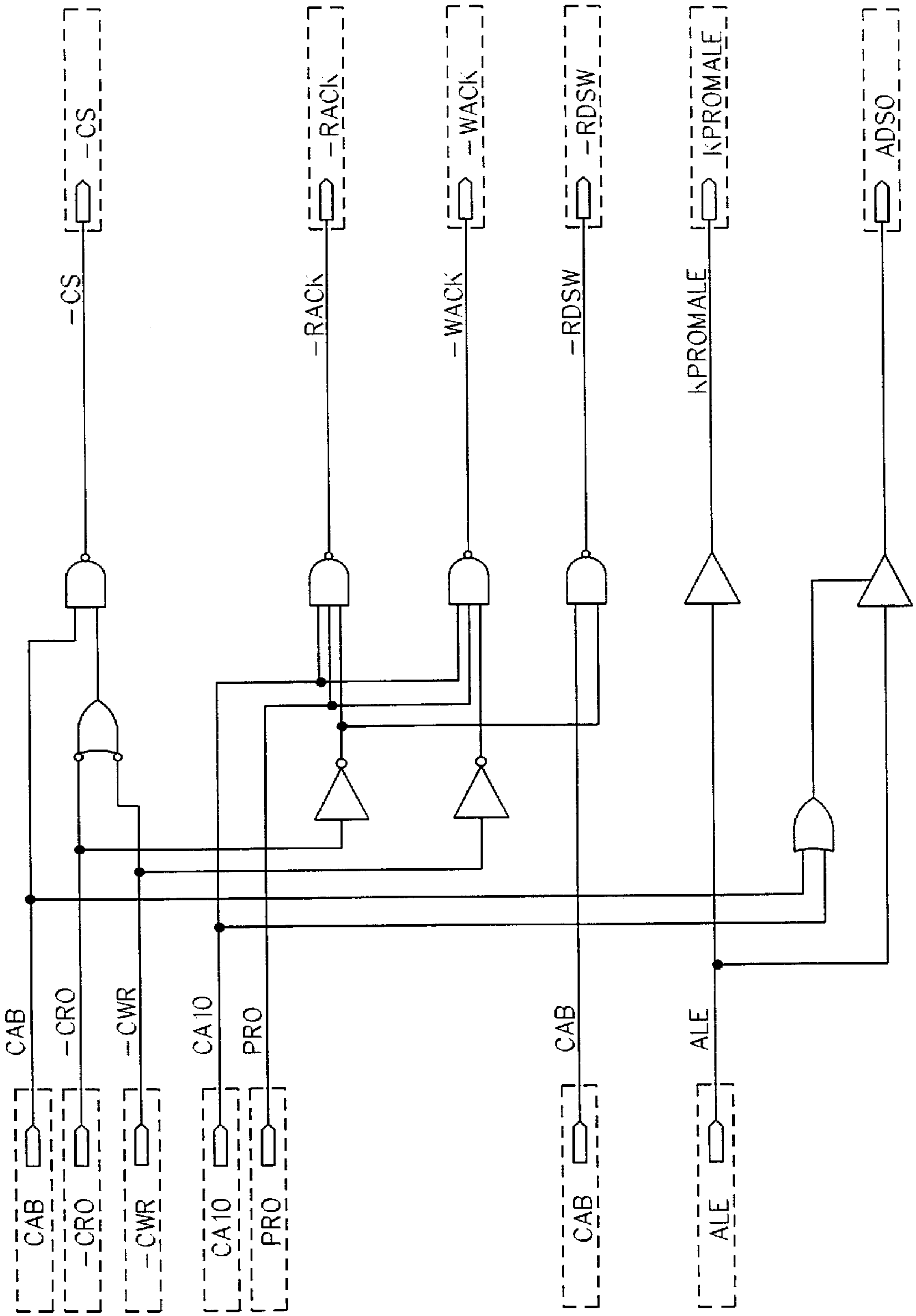
To overcome RSSI technique and circuit limitations and improve reliability of power line network arbitration the present preferred embodiment of the invention avoids the use of the RSSI signal altogether, relying instead on (1) validation of distinct data preambles to test for adequate signal-to-noise ratios and (2) special modulation symbols called FSK ACK (for Frequency Shift Key Acknowledgment) for permitting multiple nodes to acknowledge (respond) simultaneously to group polls by a network master. If the signal to noise ratio is at least 12 dB, a favorable bit error rate results in detection of valid packet preamble and start byte, packet length byte, unique node address, data payload and CRC, which together assure the reception of an accurate packet. Distinctive preamble and start bytes are chosen to permit competent comparison logic to distinguish preambles from power line noise. For example, sending a series of alternating ones and zeros (AAH) followed by a 31H (i.e., 1010101010101010001) produces an acceptably unique combination for differentiating the start code from noise. Packet length bytes also provide reliable anticipation of the packet length and the end of the packet for arbitrating the next transmission by other network nodes with minimal intergap spacing. Similarly, the special FSK ACK packet described in Figure 15 permits discrimination against normal data as well as power line noise.

In relation to the detection of special FSK ACK symbols, Figure 14a illustrates several improvements over prior techniques, which are achieved by substantially increasing the IF frequency: (1) the demodulator linear frequency range is doubled, dramatically decreasing the sensitivity to the AC coupled DFSK data comparator to the temperature coefficient and mechanical tuning drifts; (2) the FSK ACKnowledgment signal detection is more robust by setting the corresponding comparator reference near a demodulator output "rail" which is also further from the DFSK carrier and noise; and (3) the IF filter is designed for flatter pass band and sharper skirts with substantially less expensive components. Extending the linear range of the quadrature demodulator transfer function (for IF frequency vs. V_{QUAD} voltage out) permits a wider range of temperature coefficient/mechanical drift and tolerance on parts from the transmitter to the receiver. Extending the frequency range of the demodulator rails also extends the FSK ACK frequency range, which is judiciously placed near or onto a rail, providing a more robust deviation in FSK ACK frequency from the DFSK carrier to help discriminate against noise in the carrier range. A DC coupled comparator (FSK data slicer) may then be employed because the rail tends to act as a limiter on V_{QUAD} as it responds to the FSK ACK frequency, permitting the FSK ACK comparator reference to be placed in the linear range next to a rail with sufficient margin to accommodate temperature coefficient drifts and noise, as illustrated in Figure 14b. Another reason the FSK comparator works well for FSK ACK detection is that the data rate of an FSK ACK signal is designed to be much lower than for DFSK data. Placing the IF at a substantially higher frequency also provides the advantage of making IF filter design more practical for obtaining wider and flatter pass bands (and sharper skirts for rejection of out of band interference) with economical commercial components.

Figure 15 illustrates how DFSK permits the compatible use of FSK to produce special characters that may be used for group acknowledgment of requests for status of slave devices in a network. At t1 to t3 normal DFSK operation at the end of a packet is illustrated with corresponding DFSK DATA. During t3 to t4 the carrier of the master drops and the noise level of the medium creates false DATA which is rejected as invalid data by the receive data controller because it does not meet the start of packet requirements for a data packet nor does it meet the FSK ACK requirements for an ACK packet. But at t4 an FSK ACK packet begins in which the unmodulated DFSK carrier is employed as one frequency f0 for a byte (t4 to t5) and the second FSK ACK frequency acts as f1 for several bytes (t5 to t6). From t6 to t7 the ACK packet returns to f0 for the length of a byte, following which carrier transmission ceases and the data and ACK signals detect the noise level of the medium at t8 to t11. No realignment bit is required in the ACK packets. By reducing the data rate (from bits to bytes or to the lowest bit rate of the network) of the ACK protocol, at least two transmissions of equal strength may be detected simultaneously, which can occur when several remote devices in a network group respond simultaneously to a group poll. Frequencies must be within 10 kHz, which for a 5 MHZ carrier is a reasonable 0.2% (2000 PPM). Commercial crystals are available with 50 ppm tolerances at low cost. It may also be noted that the judicious use of the FSK ACK symbols and protocol avoids the use of the unreliable RSSI signal for group ACKs as described herein.

Because the FSK, ACK signal permits discrimination against normal data as well as medium noise, this advantage permits an FSK ACK packet to be employed, modified or unchanged, for other signaling applications in a network or control system. For example, in a master/slave network, the FSK ACK could provide an interrupt when a slave node requires the services of a master, which reduces polling frequency. The slave node's own address could be appended to the end of the DFSK trailer on the FSK ACK packet, reducing polling operations. Or in a peer to peer system, the FSK ACK could be used to notify other users of its intent to broadcast on the medium or to pass tokens. Changing the length of the FSK portions of the FSK ACK packet could provide control or identification data to other network devices.

It is to be understood that the above described embodiments of the invention are merely indicative of the inventors' current best mode of the invention and are illustrative of numerous and varied other embodiments which may constitute applications of the principles of the invention. Such other embodiments may be readily devised by those skilled in the art without departing from the spirit or scope of this invention and it is our intent that they be deemed within the scope of our invention.


-CS
-RACK
-WACK
-RDSW
KPROMALE
ADSO
CAB
-CRO
-CWR
CA10
PRO
ALE

ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	rackl	[,130]		130	<,0> <,0>	83902A Read Strobe to -ACK Low (2*bcyc + 30) only 2 wait states allowed
2	C	rackh	[,30]		30	<,0>	83902A Read Strobe to -ACK High
3	C	ackdv	[,55]		55	<,0>	83902A Acknowledge Low to Data Valid
4	C	rdz	[15,70]	15	70	<54.67,0.33>	83902A Read Strobe to Data TRI-STATE
5	C	ww	[50,]	50		<0,>	83902A Write Strobe Width from -ACK
6	C	rwds	[20,]	20		<0,>	83902A Register Write Data Setup
7	C	rwdh	[21,]	21		<0,>	83902A Register Write Data Hold
8	C	wackh	[,30]		30	<,0>	83902A Write High to -ACK High
9	C	wackl	[,130]		130	<,0>	83902A Write Low to -ACK Low
10	C	rsrs	[10,]	10		<0,>	83902A Register Select to Read Setup
11	C	rsrh	[0,]	0		<2.77,>	83902A Register Select Hold from Read
12	C	rswh	[0,]	0		<1.87,>	83902A Register Select Hold from Write
13	C	rsws	[15,]	15		<0,>	83902A Register Select to Write Setup (assumes ADSO high when RA lines)
14	C	bch	[20,]	20		<5,>	83902A Bus Clock High Time
15	C	bcl	[20,]	20		<5,>	83902A Bus Clock Low Time
16	C	asds	[,30]		30	<,0>	83902A Address Strobe to Data Strobe (bcl+10)
17	C	bcrl	[,43]		43	<,0>	83902A Bus Clock to Read Strobe Low
18	C	bcrh	[,40]		40	<,0>	83902A Bus Clock to Read Strobe High
19	C	avrh	[132,]	132		<0,>	83902A Address Valid to Read Strobe High

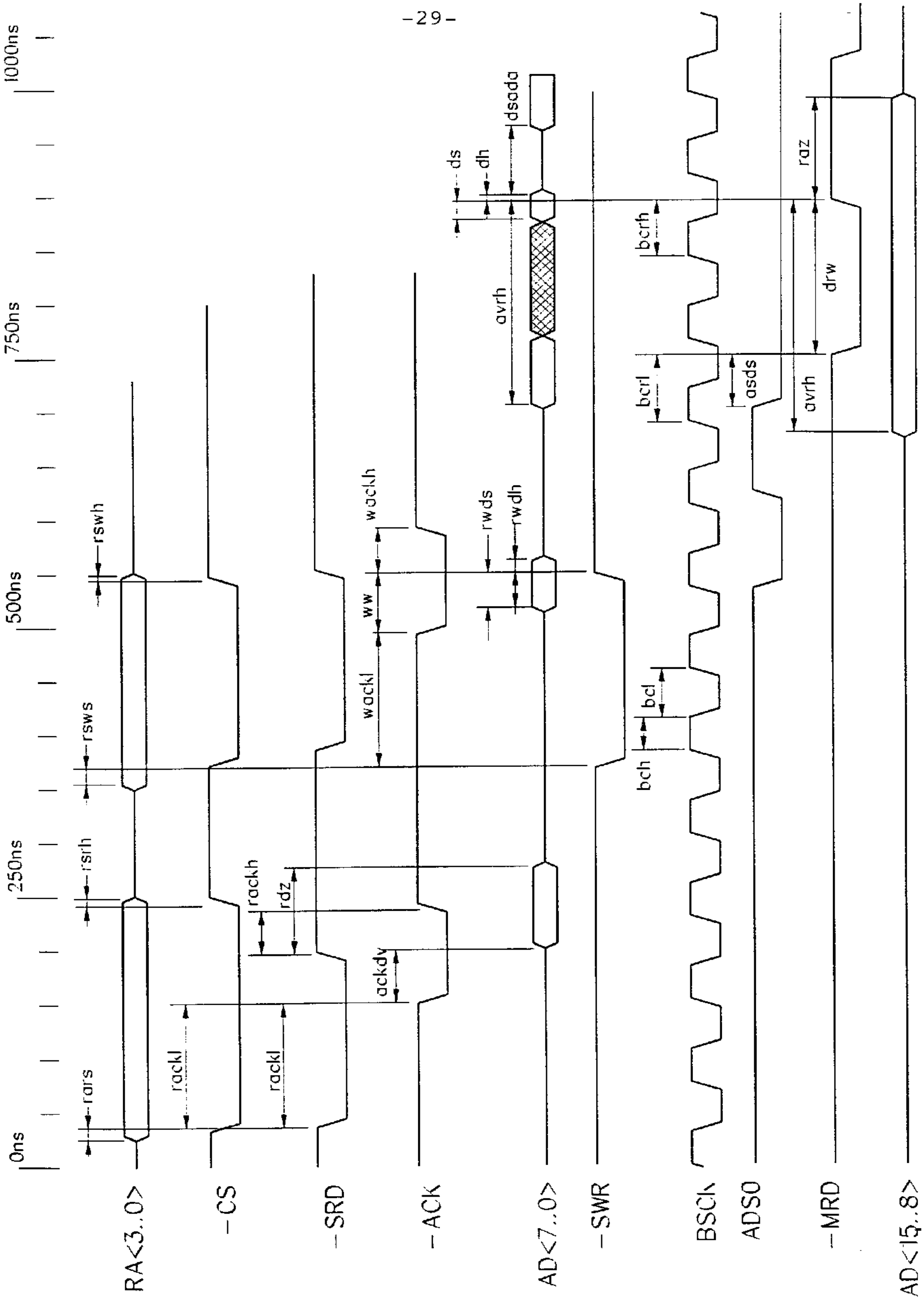
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
20	C	avrh	[132,]	132		<0,>	83902A Address Valid to Read Strobe High
21	C	ds	[22,]	22		<0,>	83902A Data Setup to Read Strobe High
22	C	drw	[85,]	85		<12,>	83902A DMA Read Strobe Width Out
23	C	dh	[0,]	0		<3,>	83902A Data Hold from Read Strobe High
24	C	dsada	[40,]	40		<0,>	83902A Data Strobe to Address Active
25	C	raz	[90,]	90		<0,>	Memory Read High to Address TRI-STATE

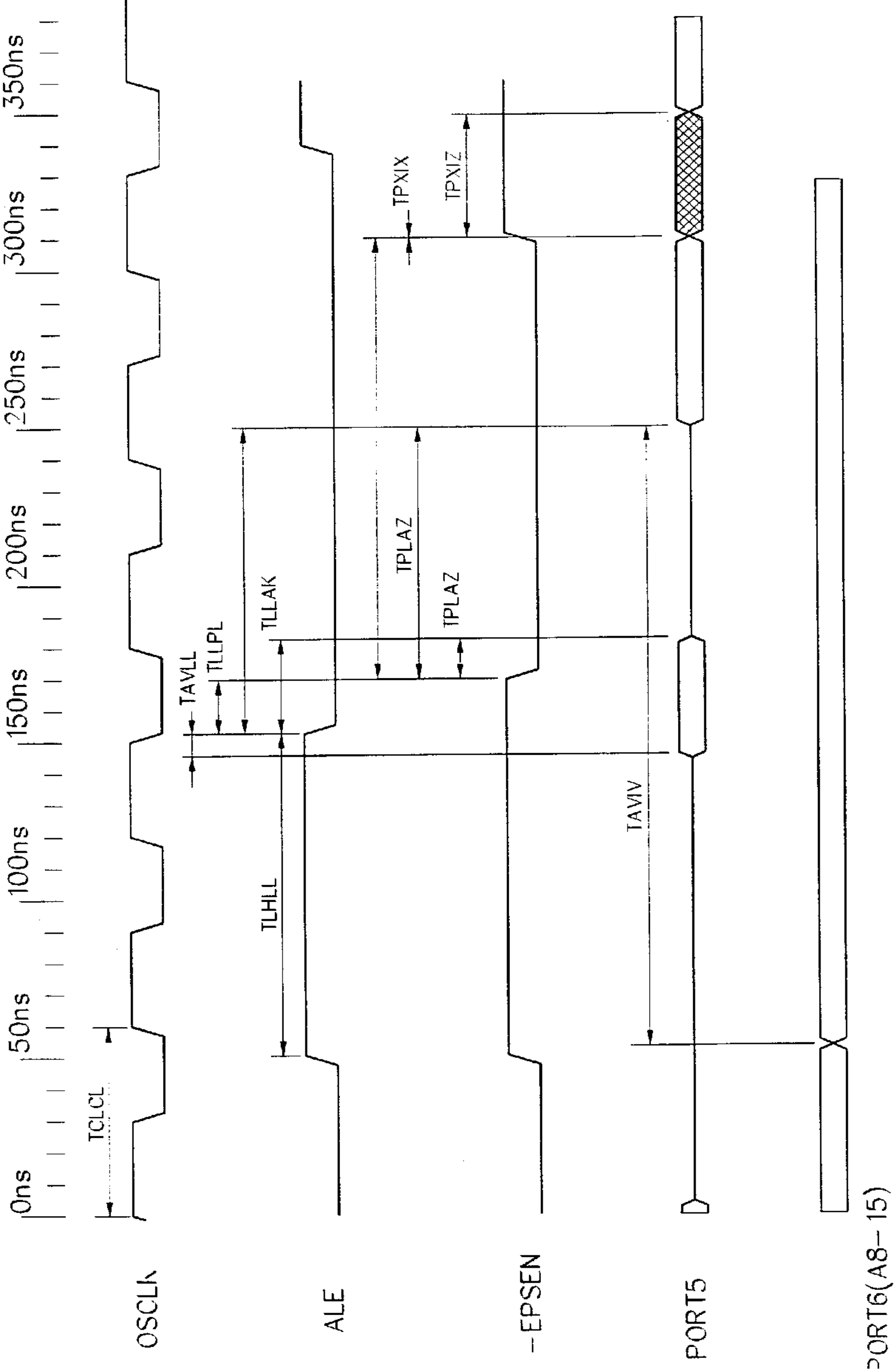
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2°TCLCL)-40)),]	81.21		<21.49,>	8X152 ALE PULSE WIDTH
2	C	tLL	[50,]	50		<52.70,>	8764 Chip DeSelect Width (87C64-1)
3	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
4	C	TCLCL	[60.61,]	60.61		<0,>	8x152 OSCILLATOR CLOCK PERIOD
5	C	TAVLL	[min((TCLCL-55)),]	5.61		<0,>	8X152 Address Valid to ALE Low
6	C	tAL	[25,]	25		<-19.39,>	8764 Address to -CE Latch Set-up
7	C	TLLAX	[min((TCLCL-35)),]	25.61		<5,>	8X152 Address Hold After ALE Low
8	C	tLA	[30,]	30		<0.61,>	8764 Address Hold from -CE Latch
9	C	TLLIV	[,min(((4°TCLCL)-100))]		142.42	<,45.41>	8X152 ALE Low to Valid Instruction In
10	C	tACL	[,150]		150	<,52.99>	8764 CE Latch Access Time
11	C	TLLPL	[min((TCLCL-40)),]	20.61		<0,>	8X152 ALE Low to -EPSEN Low
12	C	tCOE	[30,]	30		<-9.39,>	8764 ALE/-CE to Output Enable
13	C	TPLPH	[min(((3°TCLCL)-45)),]	136.82		<0.>	-EPSEN Pulse Width

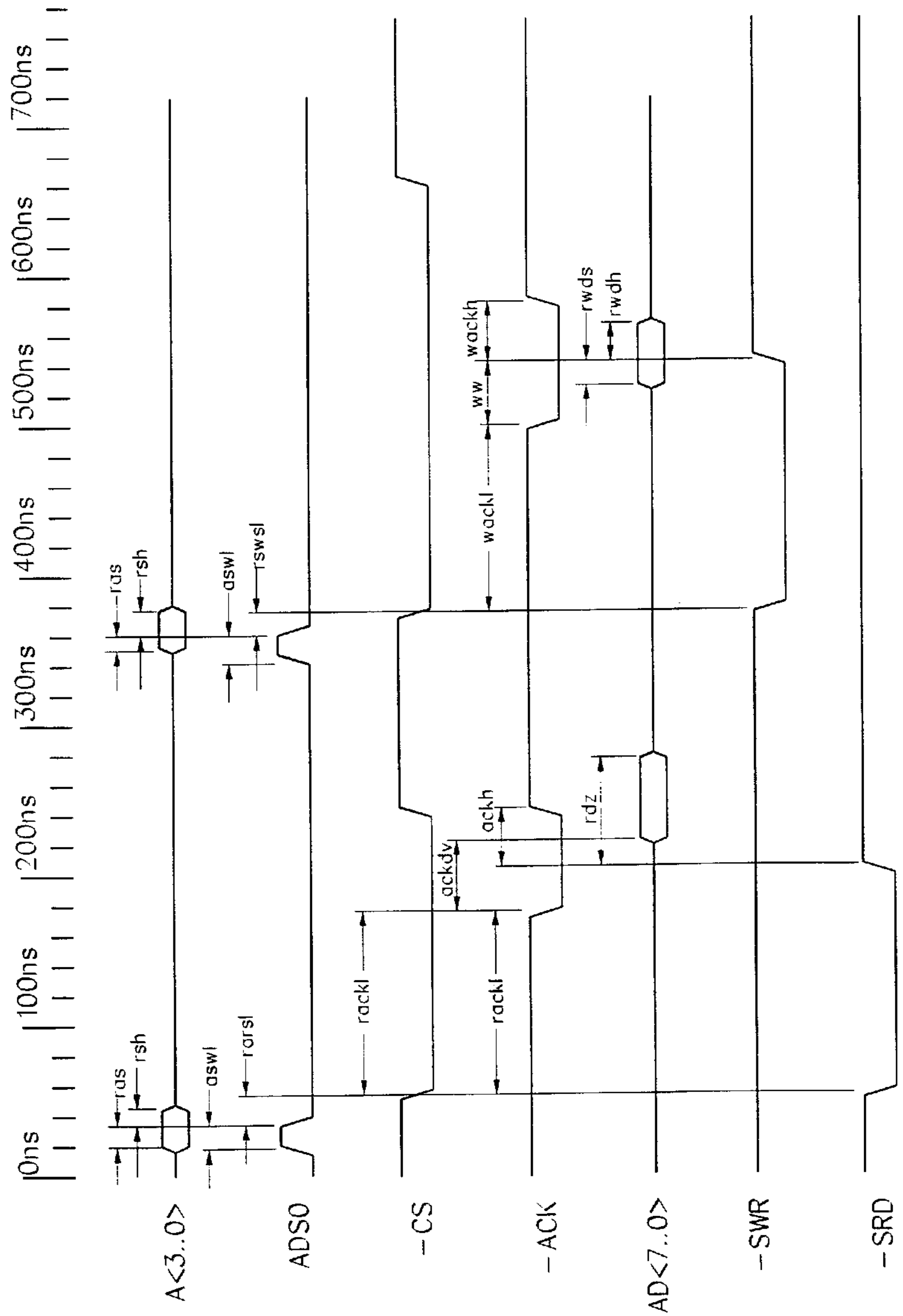
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2°T CLCL)-40)),]	81.21		<21.49,>	8X152 ALE PULSE WIDTH
2	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
3	C	TCLCL	[60.61,]	60.61		<0,>	8x152 OSCILLATOR CLOCK PERIOD
4	C	TAVLL	[min((TCLCL-55)),]	5.61		<0,>	8X152 Address Valid to ALE Low
5	C	TLLAX	[min((TCLCL-35)),]	25.61		<5,>	8X152 Address Hold After ALE Low
6	C	TLLIV	[,min(((4°T CLCL)-100))]		142.42	<,45.41>	8X152 ALE Low to Valid Instruction In
7	C	TLLPL	[min((TCLCL-40)),]	20.61		<0,>	8X152 ALE Low to -EPSEN Low
8	C	TPLPH	[min(((3°T CLCL)-45)),]	136.82		<0,>	-EPSEN Pulse Width
9	C	TPLIV	[,min(((3°T CLCL)-105)))]		76.82	<,0.4>	8X152 -EPSEN Low to Valid Instruction In
10	C	TPLAZ	[,10]		10	<,0>	8X152 -EPSEN Low to Address Float
11	C	TPXIX	[0,]	0		<0,>	8X152 Input Instruction Hold After -EPSEN
12	C	TPXIZ	[,min(((5°T CLCL)-25))]		278.03	<,242.43>	8X152 Input Instruction Float After - EPSEN
13	C	TAVIV	[,min(((5°T CLCL)-105))]		198.03	<,0>	8X152 Address to Valid Instruction In

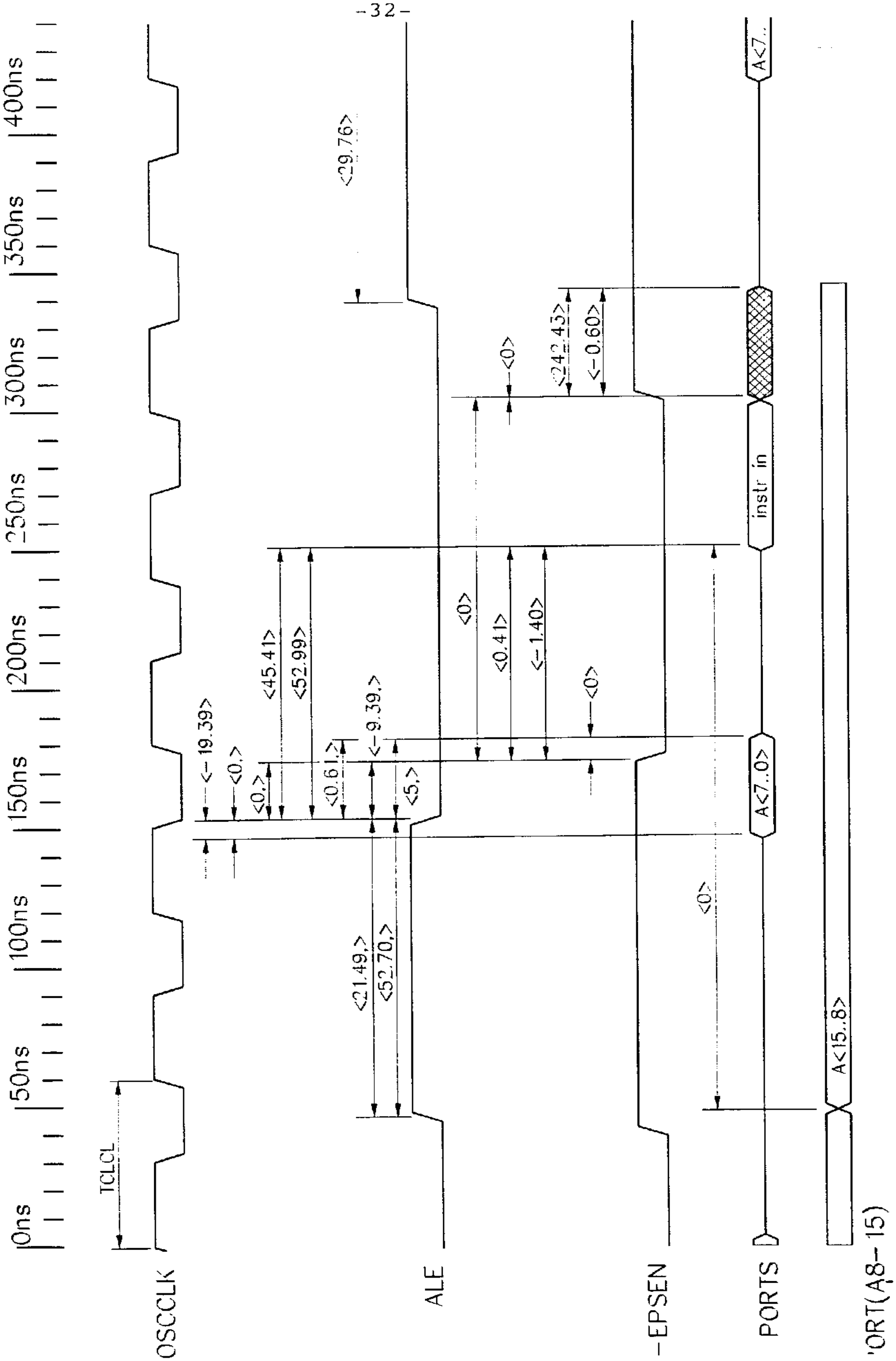
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
1	C	TLHLL	[min(((2°T CLCL)-40)),]	81.21		<0,>	8X152 ALE PULSE WIDTH
2	V	TCLCL	[60.61,]	60.61			8X152 OSCILLATOR CLOCK PERIOD
3	C	TCLCL	[60.61,]	60.61		<0,>	8x152 OSCILLATOR CLOCK PERIOD
4	C	TAVLL	[min((TCLCL-55)),]	5.61		<0,>	8X152 Address Valid to ALE Low
5	C	TLLAX	[min((TCLCL-35)),]	25.61		<0,>	8X152 Address Hold After ALE Low
6	C	TLLDV	[,max(((8° TCLCL)-150))]			<,>	8X152 ALE Low to Valid Data In
7	C	TAVDV	[,max(((9° TCLCL)-165))]			<,>	8X152 Address to Valid Data In
8	C	TWHLH	[min((TCLCL-40)),max((TCLCL+40))]	20.61		<0,>	-RD or -WR High to ALE High
9	C	TLLWL	[min(((3°TCLCL)-50)),max(((3°TCLCL)	131.82		<0,> <0,>	8X152 ALE Low to -RD or -WR Low
10	C	TRLRH	[min(((6°TCLCL)-100)),]	263.64		<0,>	8X152 -RD Pulse Width
11	C	TRLDV	[,max(((5° TCLCL)-165))]			<,>	8X152 -RD Low to Valid Data In
12	C	TRHDZ	[,max(((2° TCLCL)-70))]			<,>	8X152 Data Float after -RD
13	C	TRLAZ	[,0]		0	<,0>	8X152 -RD Low to Address Float
14	C	TRHDX	[0,]	0		<0,>	8X152 Data Hold after -RD
15	C	TAVWL	[min(((4°TCLCL)-130)),]	112.42		<25.01,>	8X152 Address to -RD or -WR Low

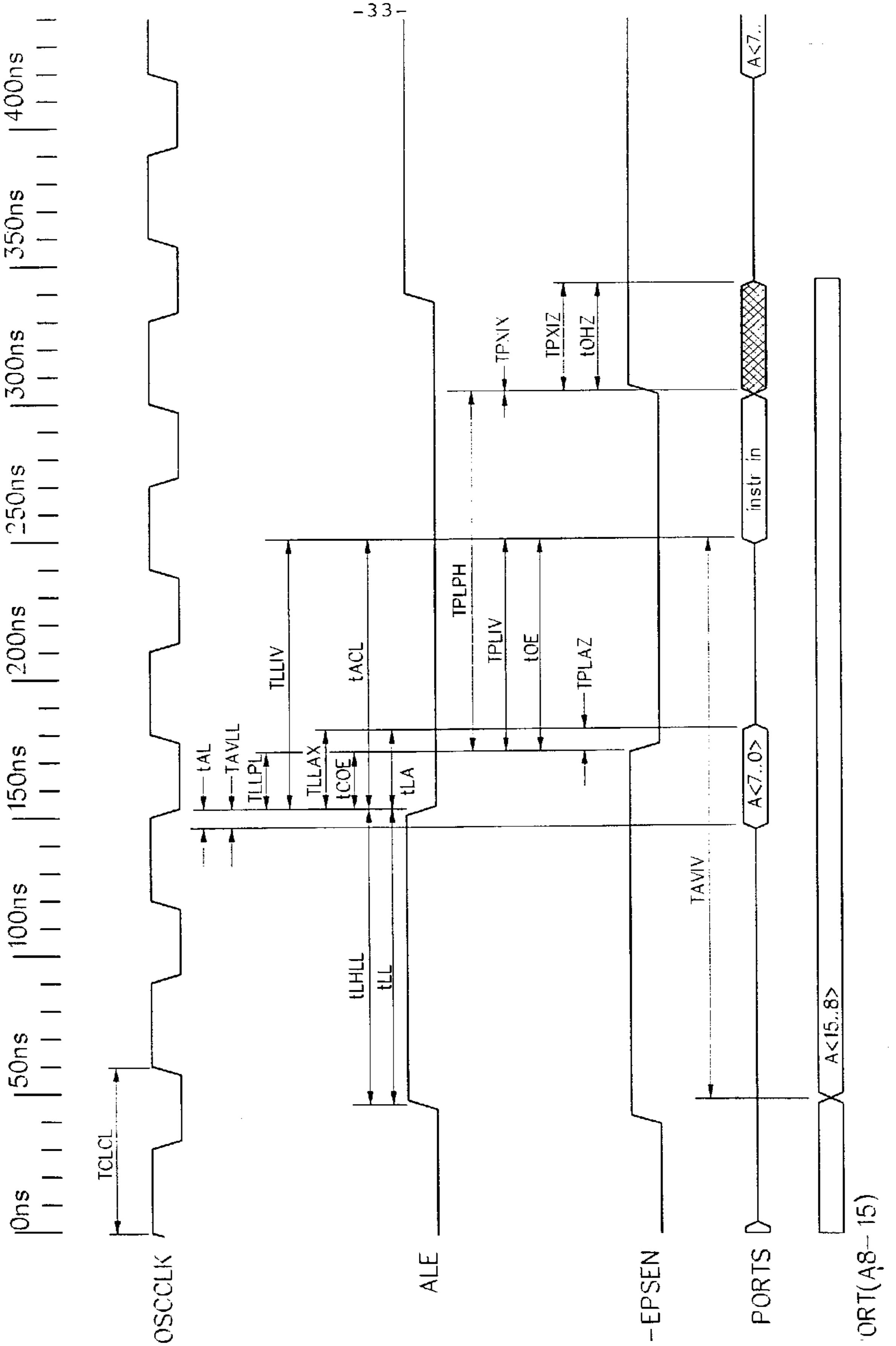
ROW		NAME	FORMULA	MIN	MAX	MARGIN	COMMENT
16	C	TWLWH	[min(((6°T CLCL)-100)),]	263.64		< 0,>	8X152 -WR Pulse Width

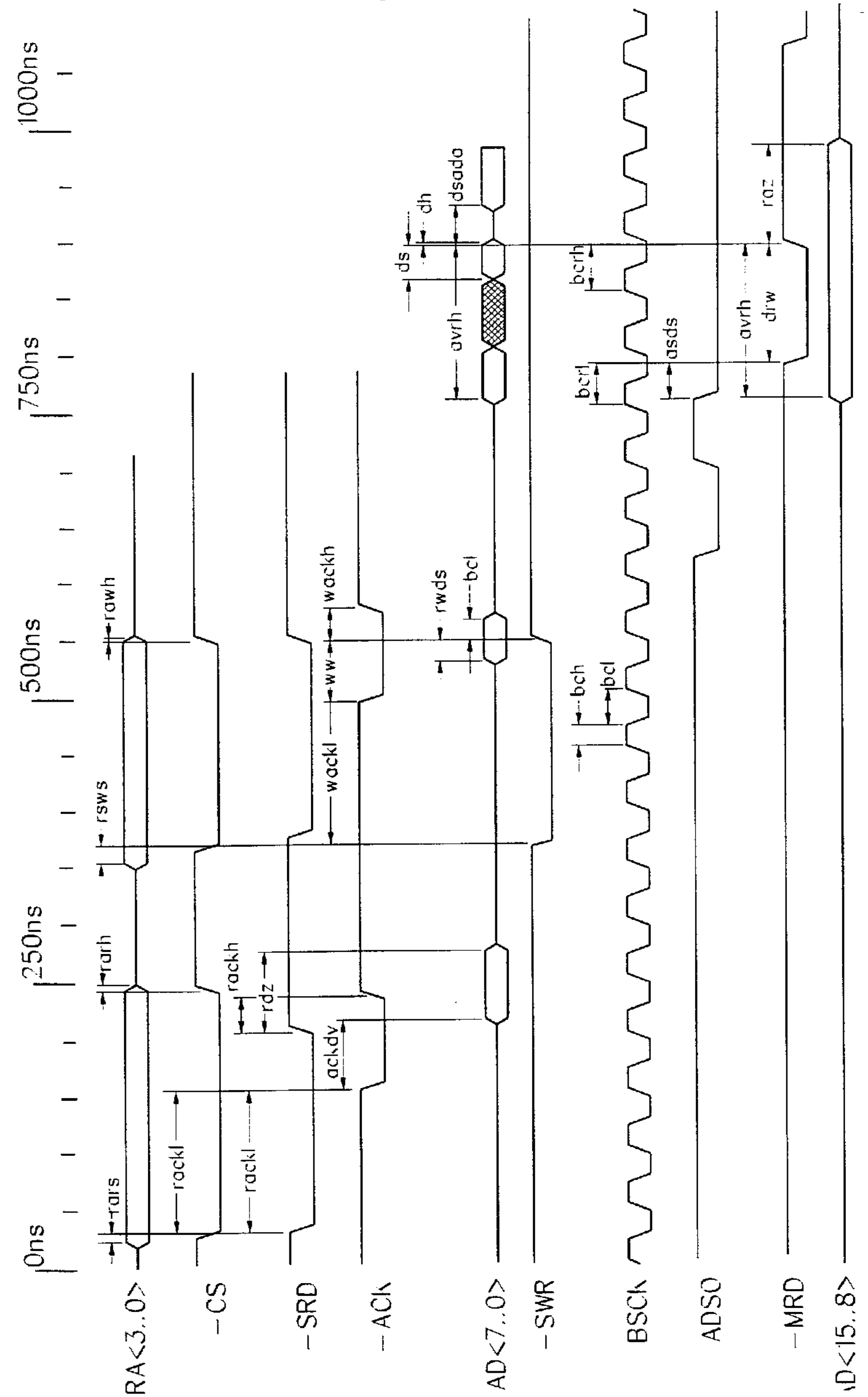

0ns
250ns
500ns
750ns
1000ns
RA<3..0>
-CS
-SRD
-ACK
AD<7..0>
-SWR
BSCK
ADS0
-MRD
AD<15..8>
rars
rackl
rackl
rsrh
rackh
rdz
ackdv
rsws
rswh
wackl
ww
wackh
rwds
rwdh
bch
bcl
bcrl
asds
avrh
avrh
bcrh
drw
raz
ds
dh
dsada

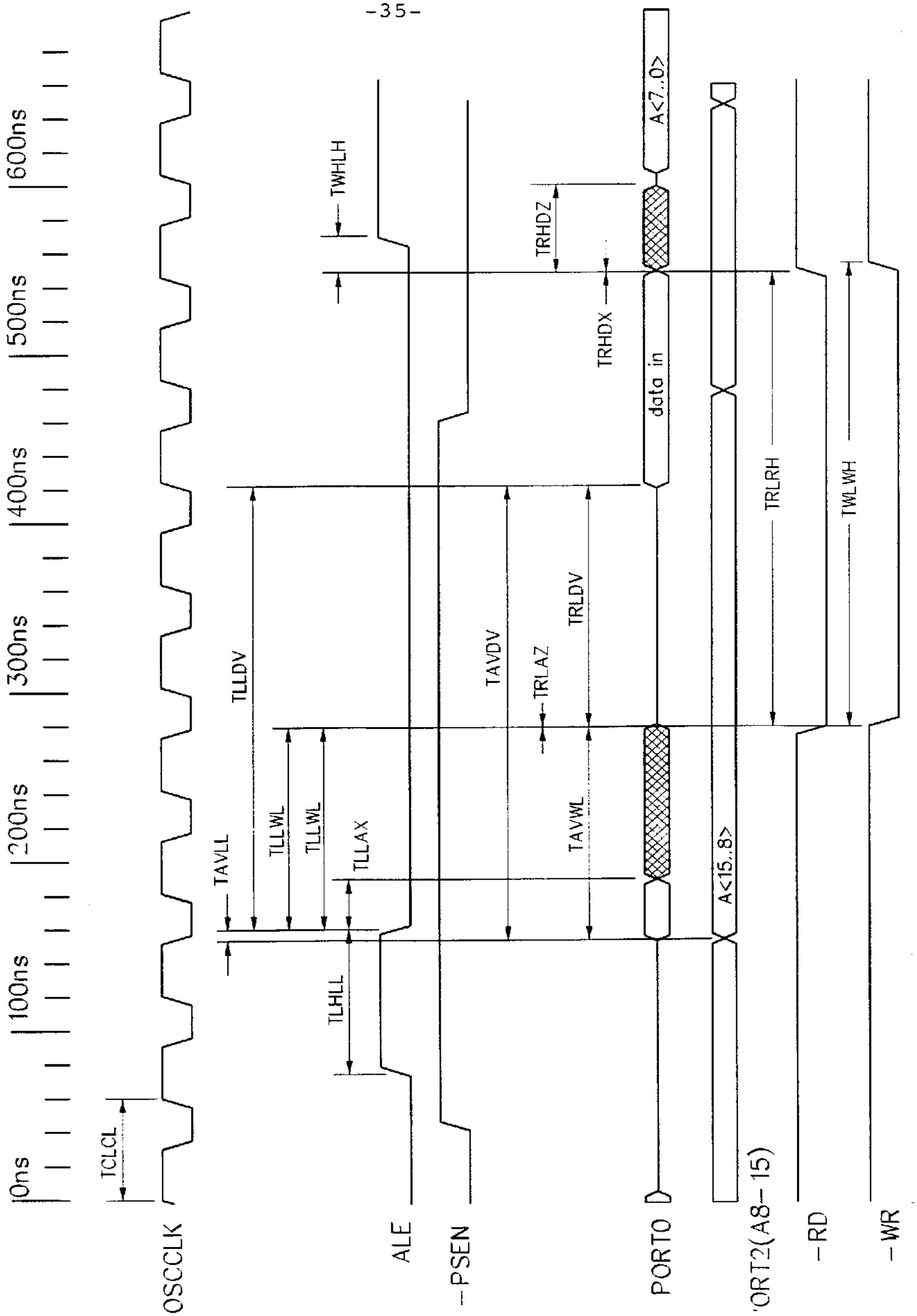

0ns
50ns
100ns
150ns
200ns
250ns
300ns
350ns
TCLCL
TLHLL
TAVLL
TLLPL
TLLAK
TPLAZ
TPLAZ
TPXIX
TPXIZ
TAVIV
ALE
-EPSEN
PORT5


0ns
100ns
200ns
300ns
400ns
500ns
600ns
700ns
A<3..0>
ADSO
-CS
-ACK
AD<7..0>
-SWR
-SRD
ras
rsh
aswl
rarsl
rackl
rackl
ackdv
ackh
rdz
ras
rsh
aswl
rswsl
wackl
ww
wackh
rwds
rwdh


0ns
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
TCLCL
OSCCLK
ALE
-EPSEN
PORTS
'ORT(A8-15)
A<7..0>
instr in
A<7..
A<15..8>
<21.49,>
<52.70,>
<-19.39>
<0,>
<0,>
<45.41>
<52.99>
<0.61,>
<-9.39,>
<5,>
<0>
<0.41>
<-1.40>
<0>
<0>
<0>
<242.43>
<-0.60>
<29.76>


0ns
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
OSCCLK
ALE
-EPSEN
PORTS
ORT(A8-15)
TCLCL
tLHLL
tLL
tAL
TAVLL
TLLPL
TLLAX
tCOE
tLA
TLLIV
tACL
TPLPH
TPLIV
tOE
TPLAZ
TAVIV
TPXIX
TPXIZ
tOHZ
A<7..0>
instr in
A<7..
A<15..8>


0ns
250ns
500ns
750ns
1000ns
RA<3..0>
-CS
-SRD
-ACK
AD<7..0>
-SWR
BSCK
ADSO
-MRD
D<15..8>
rars
rackl
rackl
ackdv
rarh
rackh
rdz
rsws
wackl
ww
wackh
rawh
rwds
bcl
bch
bcl
avrh
ds
dh
dsada
bcrl
bcrh
asds
avrh
drw
raz


0ns
100ns
200ns
300ns
400ns
500ns
600ns
OSCCLK
ALE
-PSEN
PORT0
PORT2(A8-15)
-RD
-WR
TCLCL
TLHLL
TAVLL
TLLDV
TLLWL
TLLWL
TLLAX
TAVDV
TRLAZ
TAVWL
TRLDV
TRHDX
TRHDZ
TWHLH
TRLRH
TWLWH
A<15..8>
data in
A<7..0>

WHAT IS CLAIMED IS:

1. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, each comprising:

a. an interface, connecting said repeater to an AC power line;

b. a transceiver, electrically connected to said coupler for receiving data from said coupler, wherein said transceiver further comprises:

i. a data modulator to convert digital data to analog data;

ii. a transmitter to receive the analog data from said data modulator and prepare the analog data for transmission on the power lines;

iii. a transmit filter receiving the analog data from said transmitter and filtering the resulting analog signal to transmission on the power lines;

iv. a receiver filter receiving an analog signal from the power lines;

v. a receiver receiving the filtered analog signal from said receiver filter and demodulating and digitizing said analog signal, wherein said demodulation incorporates frequency shift key (FSK) and differential frequency shift key (DFSK) technology; and

vi. a data buffer receiving said digitized data from said receiver;

c. controller, electronically connected to said transceiver, receiving data from said data buffer and sending data to said data modulator, to provide digital control to said transceiver; and

d. an interface electrically connected to said controller for transferring digital data to a computer.

2. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver further comprises:

a. a re-synchronizer to synchronize data received by said receiver.

3. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DSFK data detector.

4. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. an acknowledge signal created from a FSK carrier signal.

5. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DFSK edge detector.

6. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said transceiver receiver further comprises:

a. a DFSK peak detector.

7. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, as recited in Claim 1, wherein said controller further comprises:

a. a serializer/deserializer to serialize and deserialize the data as well as insert realignment bits and CRC logic.

8. A local area network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, comprising:

a. a means for coupling between a local area network and an AC power line for transmitting and receiving data;

b. a means for modulating a transmission carrier with network data and demodulating a transmission carrier to recover network data, said means including a means for performing differential frequency shift key modulation;

c. a means for providing noise immunity to the transferred data; and

d. a means for providing synchronization of the transferred data.

9. A local area network repeater system for transmitting and receiving network data between repeater, comprising a controller, wherein said controller includes a state machine which permits the selection of a wide range of data rates without requiring the modification of carrier frequency.

10. A local area computer network repeater system for transmitting and receiving network data between repeaters, the system comprising a plurality of repeaters, each comprising:

means for coupling a local area network interface to a local area computer network or network segment for transmitting a bi-directional network data stream, said data stream having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate;

means for frequency shift key modulating a transmission carrier with said network data stream and demodulating said frequency shift key modulated transmission carrier to recover network data, said frequency shift key modulated transmission carrier having an instantaneous frequency bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation, said means comprising a receiver chip which utilizes at least one stage of gain and filter, and said means providing at least about 90 decibels of gain;

means for coupling bi-directional network data between said network interface and said carrier modulation and demodulation means; and

means for coupling said transmission carrier to an AC power line to produce a power line carrier signal having a frequency in the range from about 2 to about 20 megahertz.

11. A local area network repeater system as recited in claim 1 wherein said local area network interface comprises a network interface selected from the following:

Ethernet network interface controller means;

Token ring network interface controller means;

Arcnet network interface controller means;

RS-232 interface controller means;

RS-485 network interface controller means;

Serial data, open standard interface; and

Parallel data interface.

12. A local area network repeater system as recited in claim 1 wherein said transmission carrier modulation and demodulation means further comprises transmission means selected from the following:

Time domain multiple access means wherein carrier data modulation and transmission is alternated with carrier data demodulation and data reception, said modulation and demodulation carriers operating on the same frequency; and

Frequency domain multiple access means wherein said carrier data modulation and transmission utilizes one carrier frequency and said carrier data demodulation and reception utilizes a second frequency.

13. A local area network repeater system as recited in claim 1 further comprising repeater controller means for performing control functions selected from among the following:

initializing and controlling said network interface means, as required to permit transparent repeating of network data over the AC power line;

monitoring said data modulated transmission carriers and arbitrating data transmissions to permit only one repeater at a time to transmit a carrier of a particular frequency onto the AC power line; and

attaching and removing data preambles and addresses; reformatting data, encrypting and decrypting data, and providing alternate data communications ports.

14. A repeater system for transmission of high frequency computer data signals through an AC power line, the system comprising a plurality of repeaters, each repeater comprising:

means for coupling input signals and output signals to a signal port;

carrier modulation means for frequency shift key modulating a transmission carrier with said input signals to produce a modulated signal having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated signal having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation;

demodulation means for demodulating said modulated signal to recover said output signals, said modulation means further comprising means for changing the resonant frequency produced by an oscillator in response to an input signal by driving an output port of the oscillator;

said demodulation means further comprising means for providing at least about 90 decibels of gain;

means for coupling bi-directional signals between said signal port and said carrier modulating and demodulation means; and

means for coupling said transmission carrier to the AC power line to produce a power line carrier signal having a frequency in the range from about 2 to about 20 megahertz.

15. A method for power line carrier data transmission, said method comprising the steps of:

generating a carrier signal at a frequency in the range of from about 2 to 20 megahertz;

frequency shift key modulating said carrier signal to provide a modulated carrier signal having a data bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated carrier signal having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation; and

coupling the frequency shift key modulated carrier signal onto an ac power line.

16. The method of claim 8, further comprising the steps of:

coupling the modulated carrier signal off of the AC power line; and

demodulating the carrier signal.

17. The method of claim 8, wherein said modulating step comprises modulating the carrier signal to correspond to a digital data signal.

18. The method of claim 8, wherein said modulating step comprises modulating the carrier signal to correspond to an analog data signal.

19. The method of claim 8, wherein said modulating step comprises buffering with multi-stage transmitter drivers.

20. The method of claim 9, wherein said demodulating step comprises filtering the carrier signal in stages.

21. The method of claim 8, further comprising the collision avoidance steps of:

listening for traffic on the AC power line; and

selecting between (a) transmitting an access request after detecting termination of a transmission, and (b) beginning data transmission after detecting no other traffic.

22. An embedded PLC communications system comprising a plurality of networked communications devices, each of said communications devices comprising:

an embedded microcontroller having a communication port;

carrier modulation means for frequency shift key modulating a transmission carrier with data signals from said communication port to produce a modulated carrier, said modulated carrier having a bitrate of up to 2 megabits per second and a data bandwidth approximately equal to said bitrate, said modulated carrier having an instantaneous bandwidth which is not substantially greater than the greater of either about twice said data bandwidth or the frequency deviation of said frequency shift key modulation; and

a receiver comprising a demodulator for demodulating said modulated carrier to recover corresponding data signal, said receiver comprising at least one intermediate frequency gain and filtering stage utilizing an intermediate frequency in the range from about 2 to about 20 megahertz and providing a receiver gain of at least about 90 decibels;

means for coupling said data signals between said communication port and said carrier modulation means; and

means for coupling said modulated carrier to an AC power line.

23. The system of claim 17, further comprising network arbitration and control means.

24. The system of Claim 17, wherein said means for coupling said transmission carrier to an AC power line comprises an existing AC power cord.

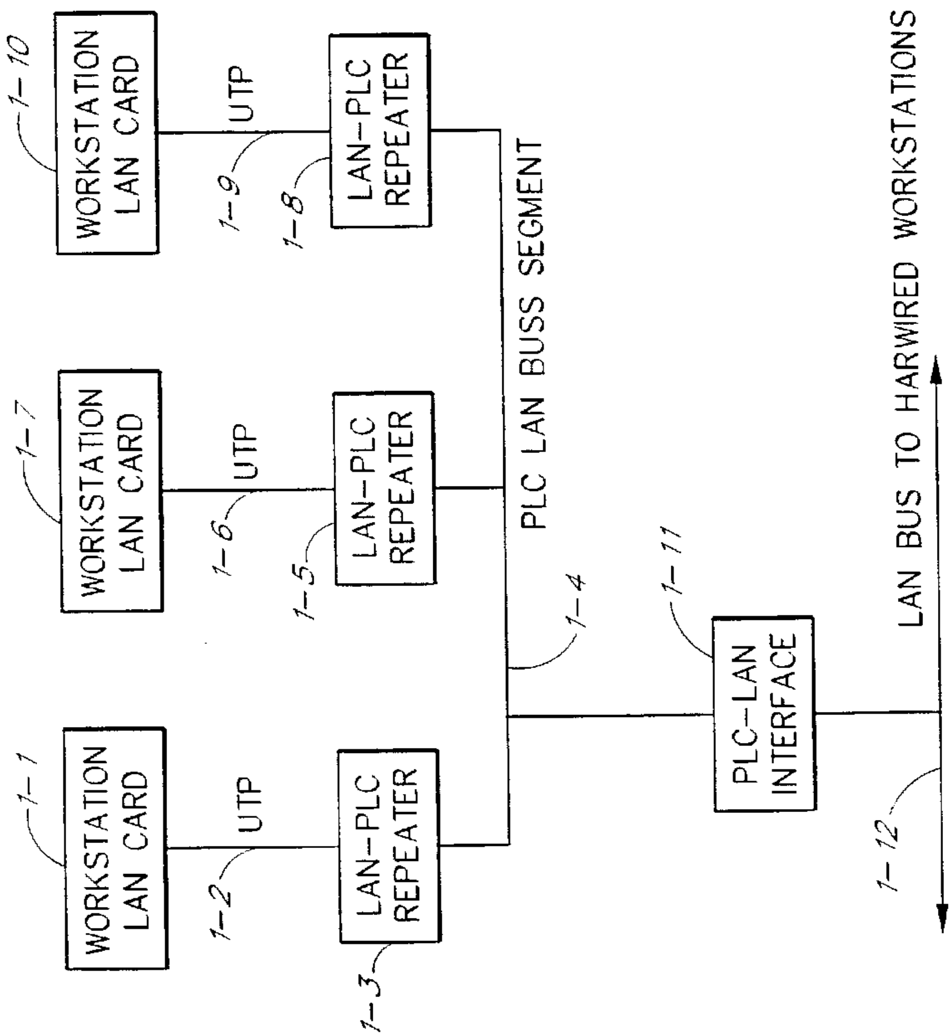

WORKSTATION LAN CARD
1-1
1-2
UTP
LAN-PLC REPEATER
1-3
WORKSTATION LAN CARD
1-7
1-6
UTP
LAN-PLC REPEATER
1-5
WORKSTATION LAN CARD
1-10
1-9
UTP
LAN-PLC REPEATER
1-8
PLC LAN BUSS SEGMENT
1-4
PLC-LAN INTERFACE
1-11
LAN BUS TO HARWIRED WORKSTATIONS
1-12

FIG. 1

2/47

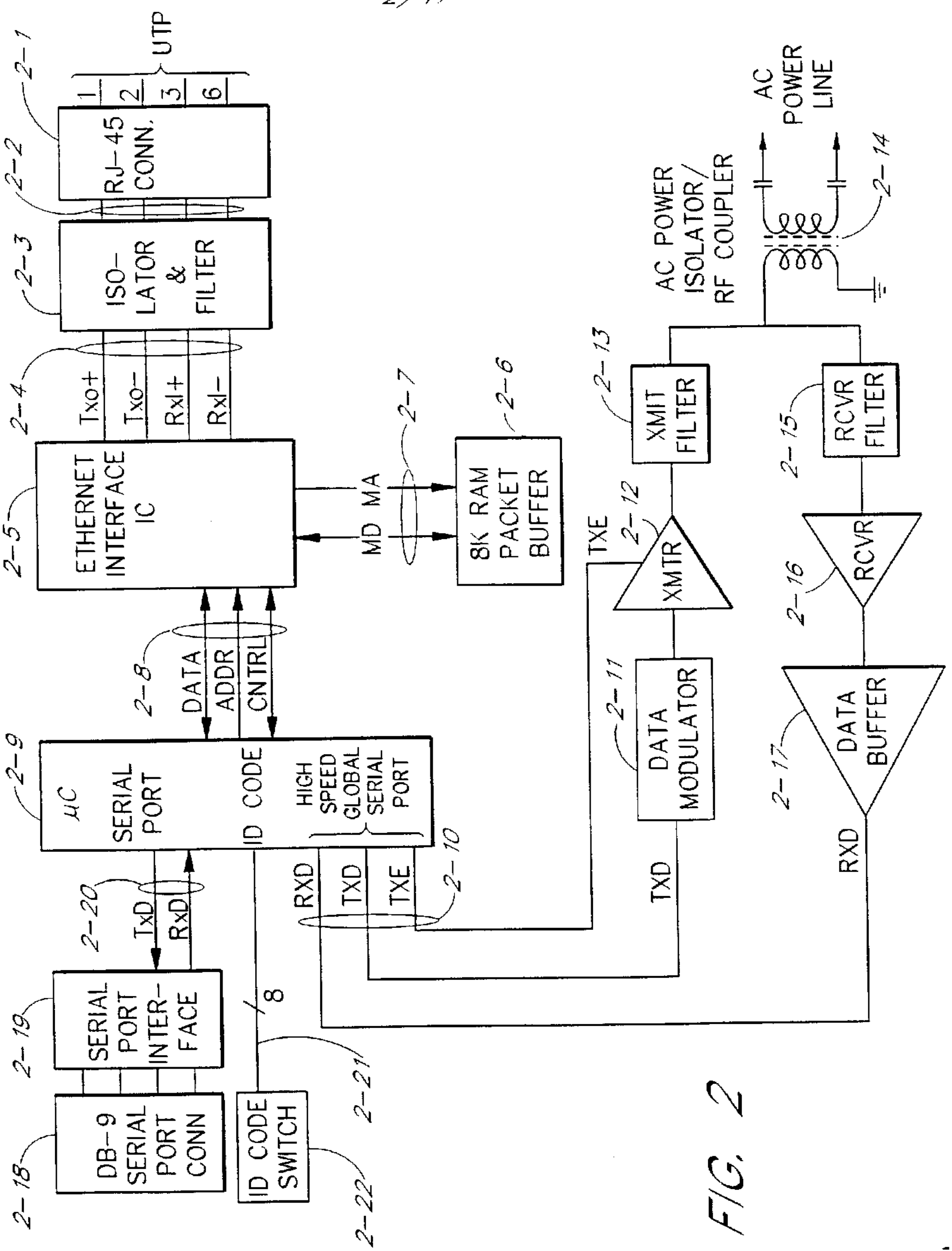

UTP
1
2
3
6
RJ-45 CONN.
ISO-LATOR & FILTER
Txo+
Txo-
RxI+
RxI-
ETHERNET INTERFACE IC
MD MA
8K RAM PACKET BUFFER
DATA
ADDR
CNTRL
μC
SERIAL PORT
ID CODE
HIGH SPEED GLOBAL SERIAL PORT
TxD
RxD
8
RXD
TXD
TXE
SERIAL PORT INTER-FACE
DB-9 SERIAL PORT CONN
ID CODE SWITCH
XMTR
XMIT FILTER
DATA MODULATOR
AC POWER ISOLATOR/ RF COUPLER
AC POWER LINE
RCVR FILTER
RCVR
DATA BUFFER
2-1
2-2
2-3
2-4
2-5
2-6
2-7
2-8
2-9
2-10
2-11
2-12
2-13
2-14
2-15
2-16
2-17
2-18
2-19
2-20
2-21
2-22

FIG. 2

3/47

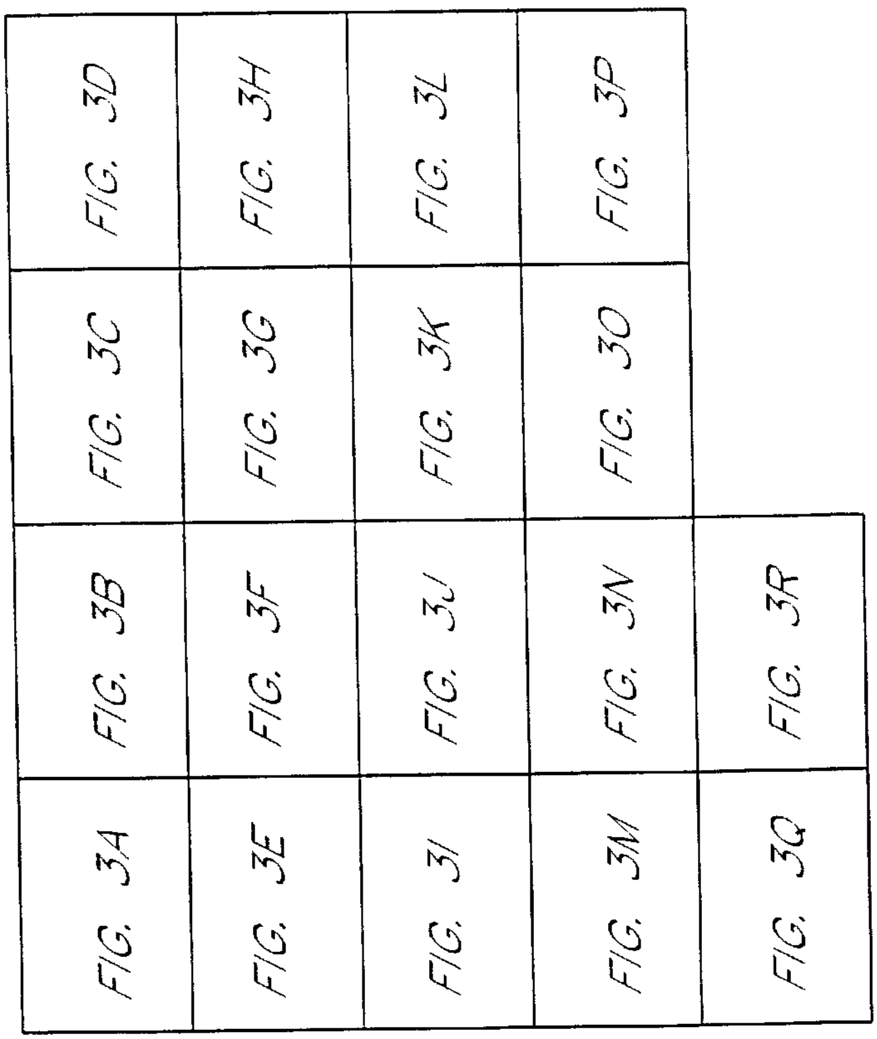


FIG. 3A
FIG. 3B
FIG. 3C
FIG. 3D
FIG. 3E
FIG. 3F
FIG. 3G
FIG. 3H
FIG. 3I
FIG. 3J
FIG. 3K
FIG. 3L
FIG. 3M
FIG. 3N
FIG. 3O
FIG. 3P
FIG. 3Q
FIG. 3R

FIG. 3

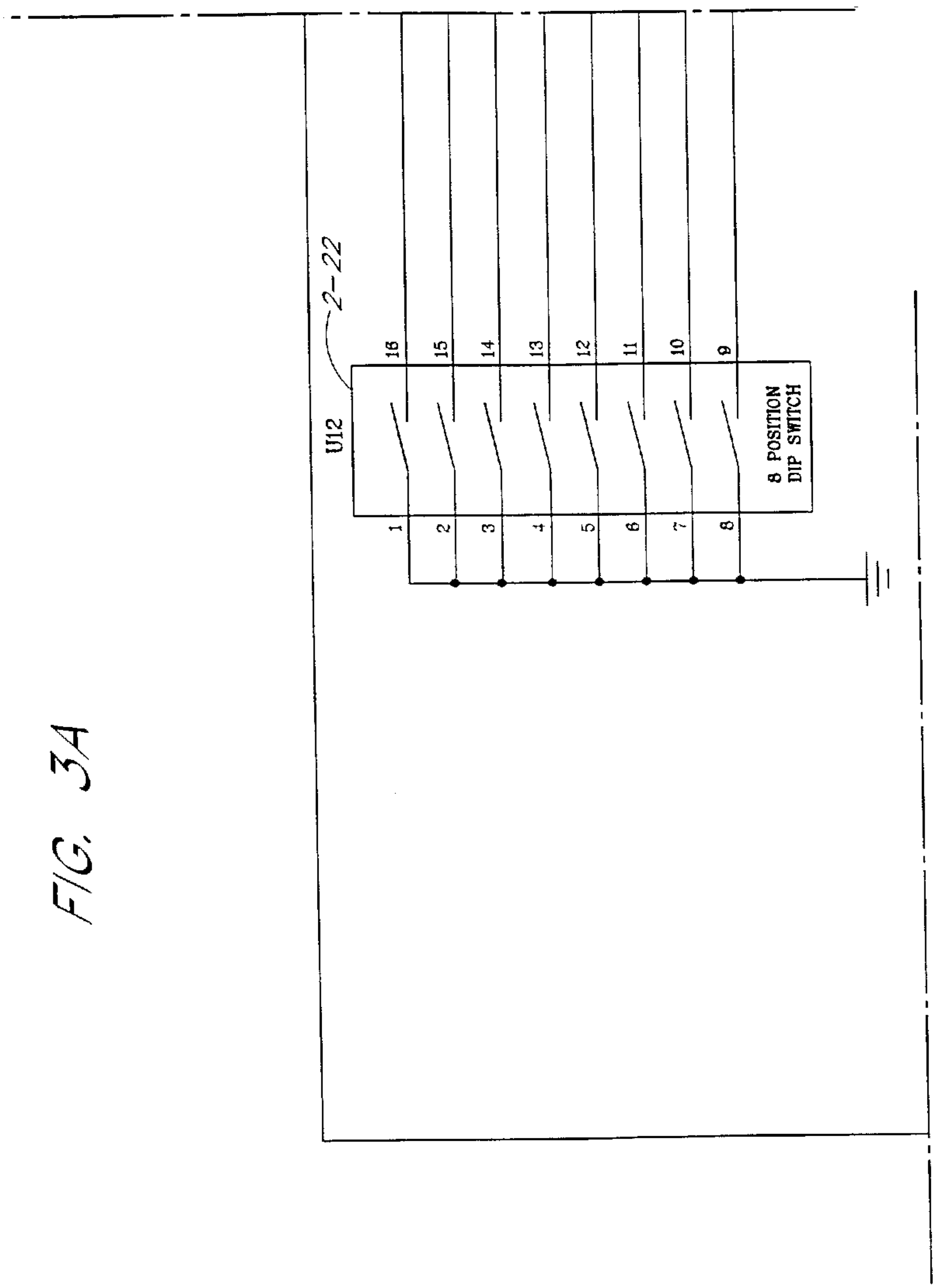


FIG. 3A

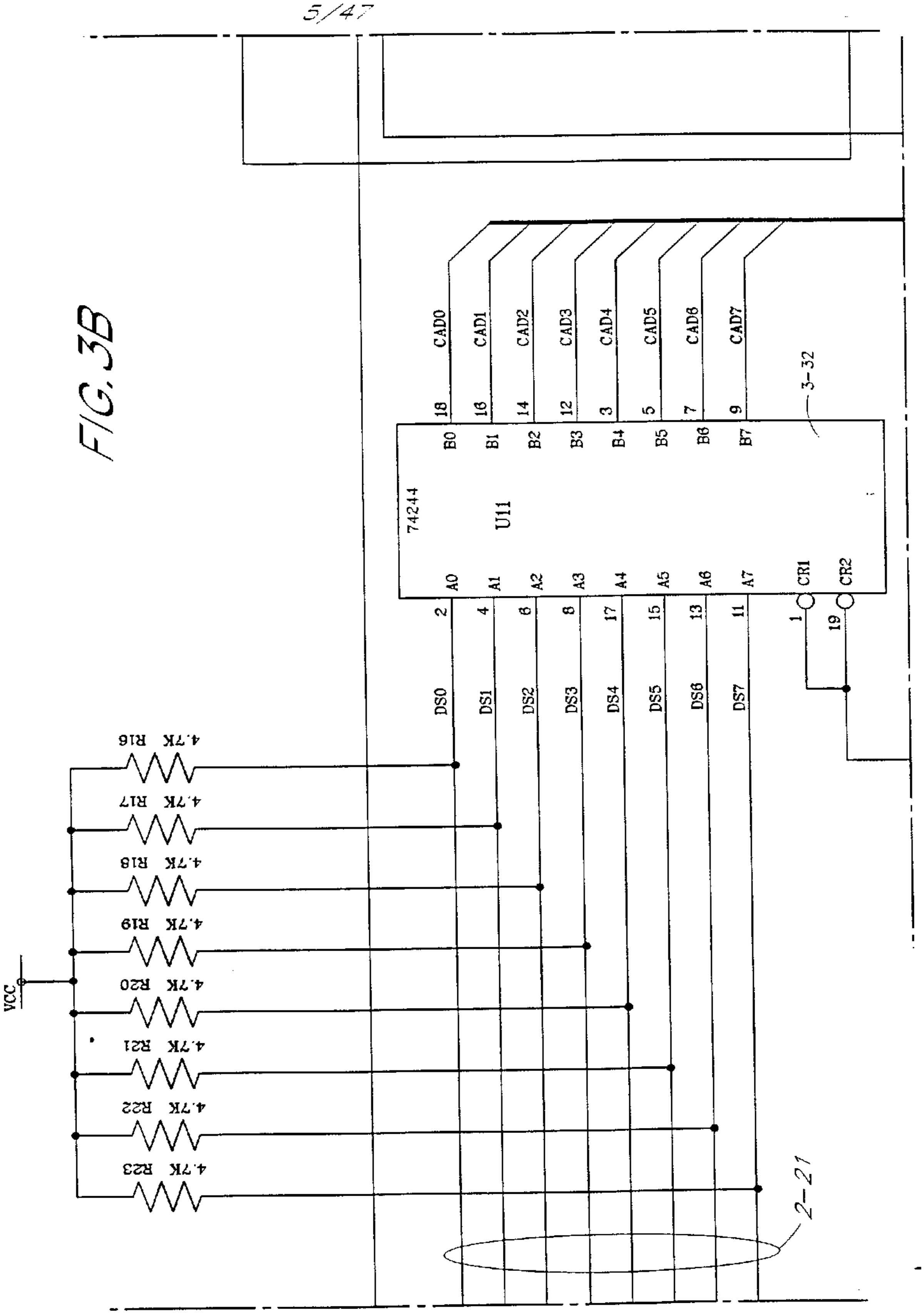
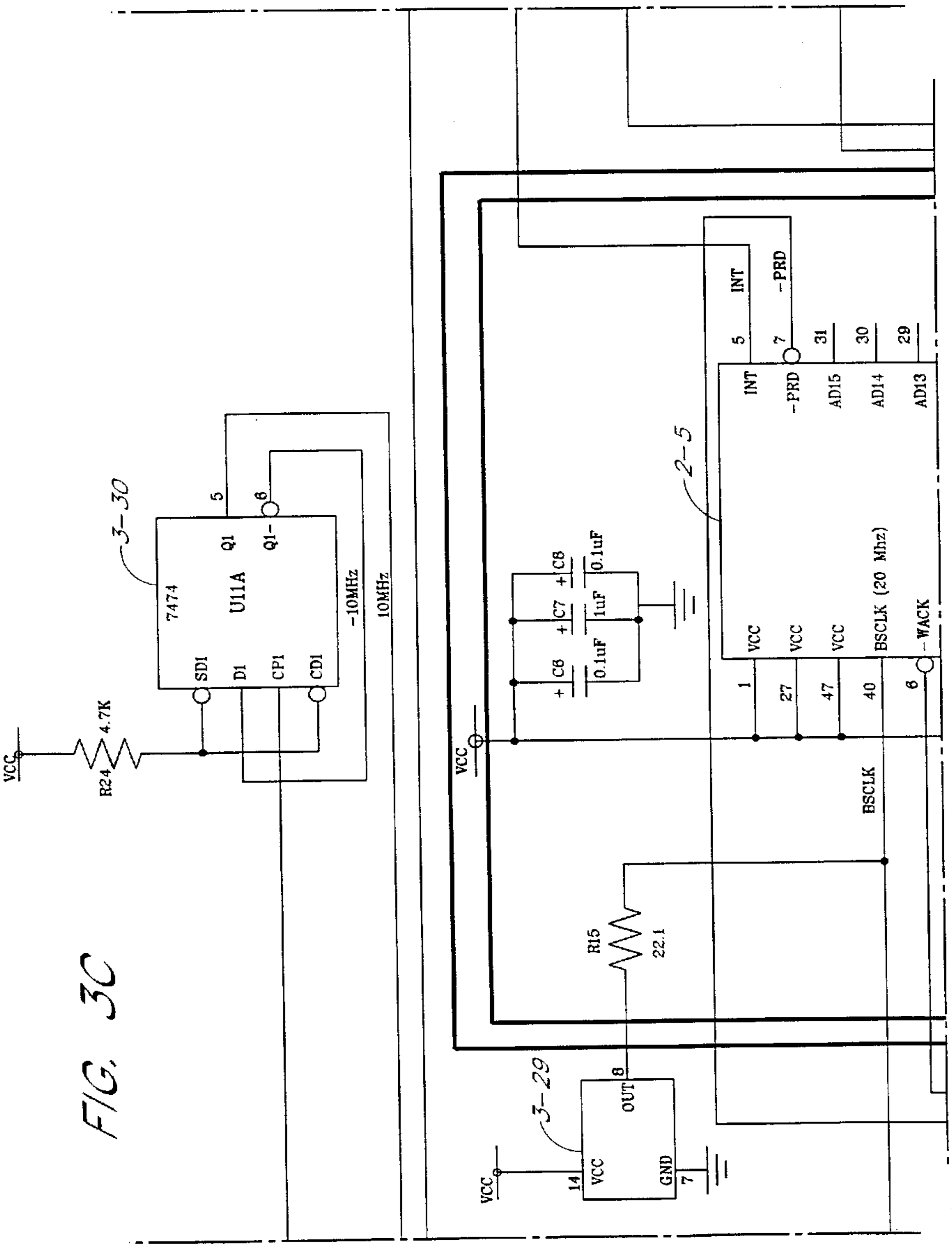

CAD0
CAD1
CAD2
CAD3
CAD4
CAD5
CAD6
CAD7
3-32
B0
B1
B2
B3
B4
B5
B6
B7
74244
U11
A0
A1
A2
A3
A4
A5
A6
A7
CR1
CR2
DS0
DS1
DS2
DS3
DS4
DS5
DS6
DS7
4.7K R16
4.7K R17
4.7K R18
4.7K R19
4.7K R20
4.7K R21
4.7K R22
4.7K R23
VCC
2-21

FIG. 3B



3-30
7474
U11A
Q1
Q1-
5
6
SDI
D1
CP1
CD1
-10MHz
10MHz
VCC
R24
4.7K
VCC
C6
C7
C8
0.1uF
1uF
0.1uF
2-5
INT
-PRD
AD15
AD14
AD13
5
7
31
30
29
VCC
VCC
VCC
BSCLK (20 Mhz)
-WACK
1
27
47
40
6
BSCLK
R15
22.1
3-29
OUT
8
VCC
14
GND
7
VCC

FIG. 3C

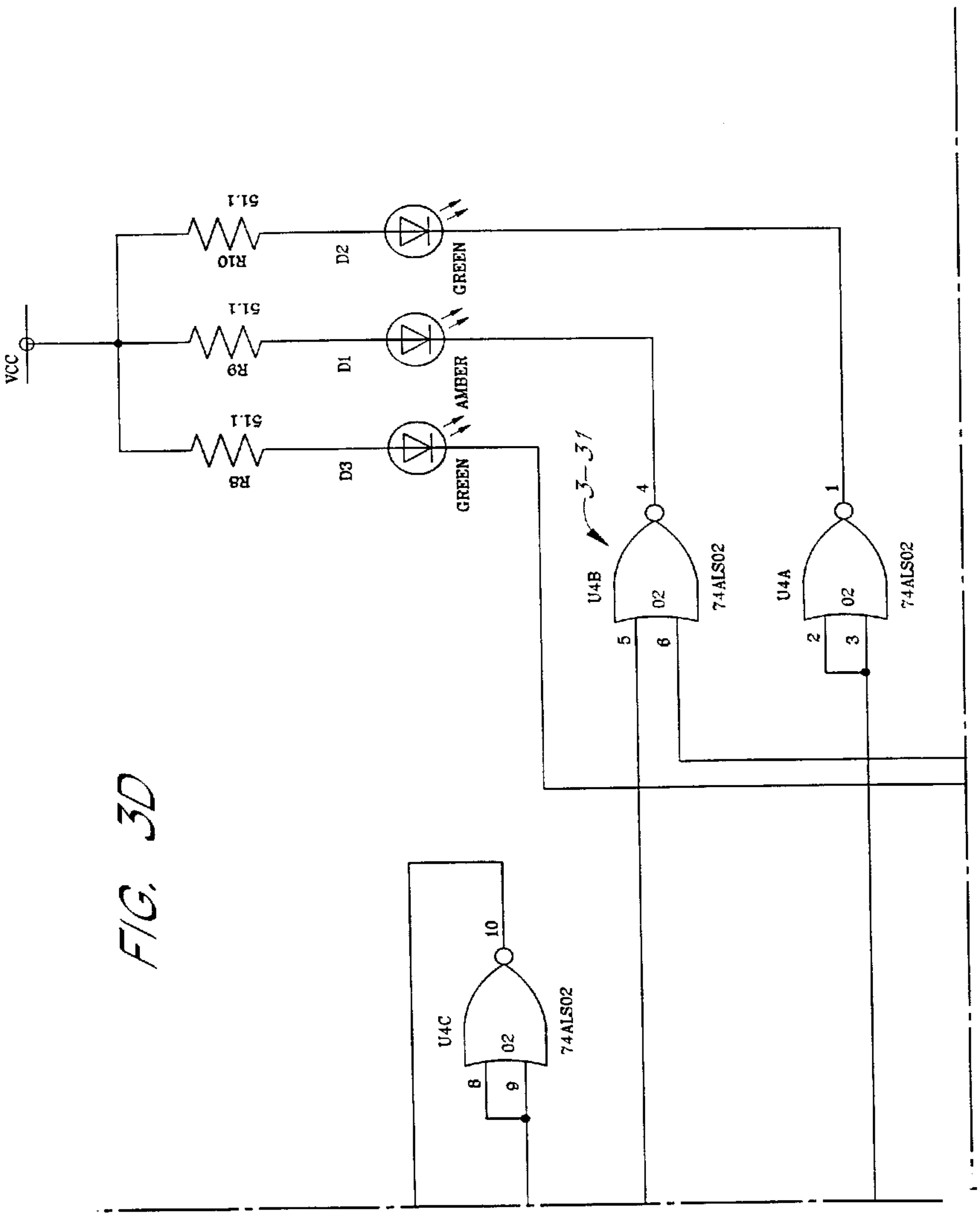

VCC
R8
R9
R10
51.1
51.1
51.1
D1
D2
D3
GREEN
AMBER
GREEN
3-31
U4A
U4B
U4C
02
74ALS02
1
2
3
4
5
6
8
9
10

FIG. 3D

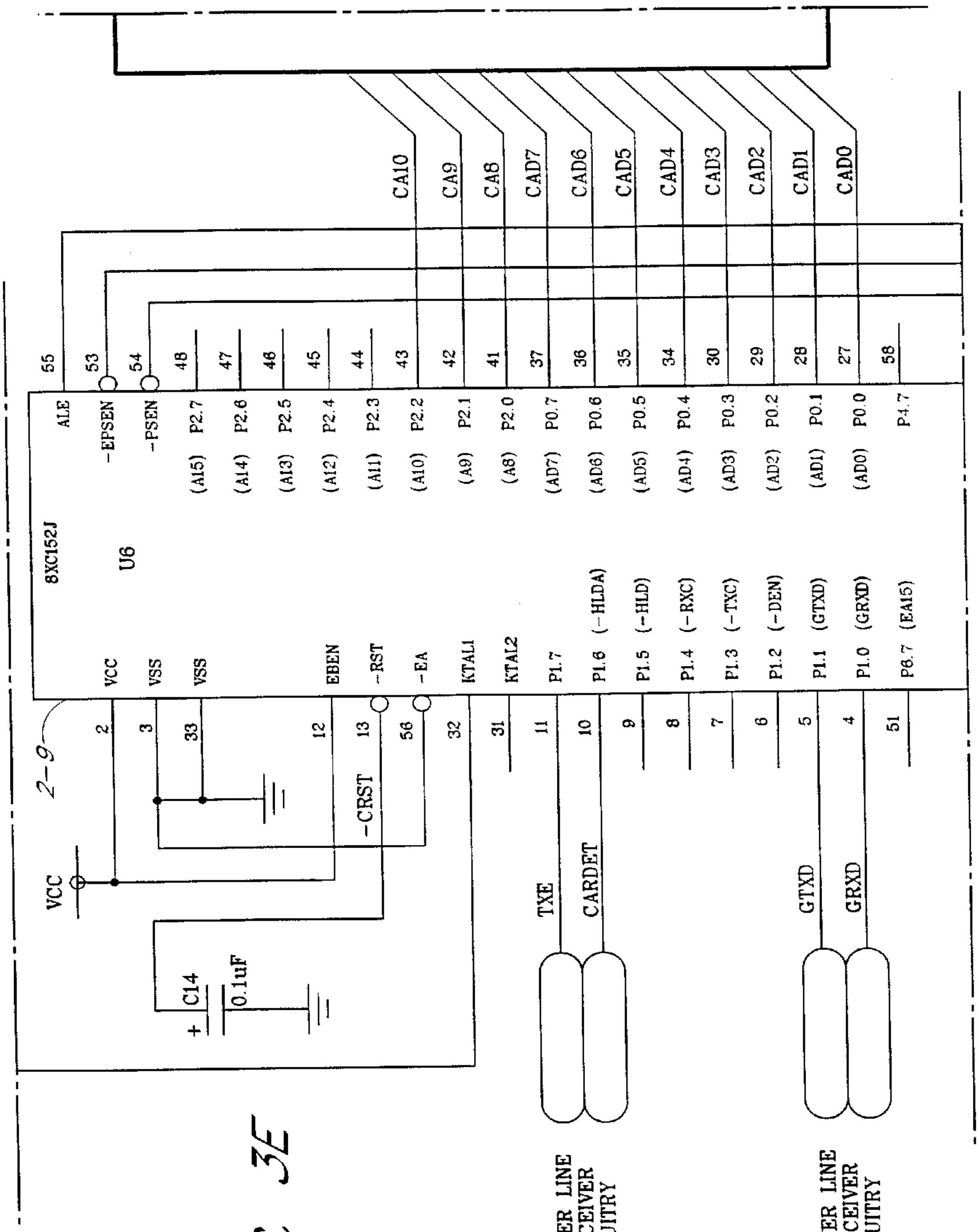

CA10
CA9
CA8
CAD7
CAD6
CAD5
CAD4
CAD3
CAD2
CAD1
CAD0
8XC152J
U6
ALE
-EPSEN
-PSEN
P2.7 (A15)
P2.6 (A14)
P2.5 (A13)
P2.4 (A12)
P2.3 (A11)
P2.2 (A10)
P2.1 (A9)
P2.0 (A8)
P0.7 (AD7)
P0.6 (AD6)
P0.5 (AD5)
P0.4 (AD4)
P0.3 (AD3)
P0.2 (AD2)
P0.1 (AD1)
P0.0 (AD0)
P4.7
55
53
54
48
47
46
45
44
43
42
41
37
36
35
34
30
29
28
27
58
VCC
VSS
VSS
EBEN
-RST
-EA
KTAL1
KTAL2
P1.7
P1.6 (-HLDA)
P1.5 (-HLD)
P1.4 (-RXC)
P1.3 (-TXC)
P1.2 (-DEN)
P1.1 (GTXD)
P1.0 (GRXD)
P6.7 (EA15)
2
3
33
12
13
56
32
31
11
10
9
8
7
6
5
4
51
2-9
-CRST
VCC
C14
0.1uF
+
TXE
CARDET
GTXD
GRXD
TO POWER LINE TRANSCEIVER CIRCUITRY
TO POWER LINE TRANSCEIVER CIRCUITRY

FIG. 3E

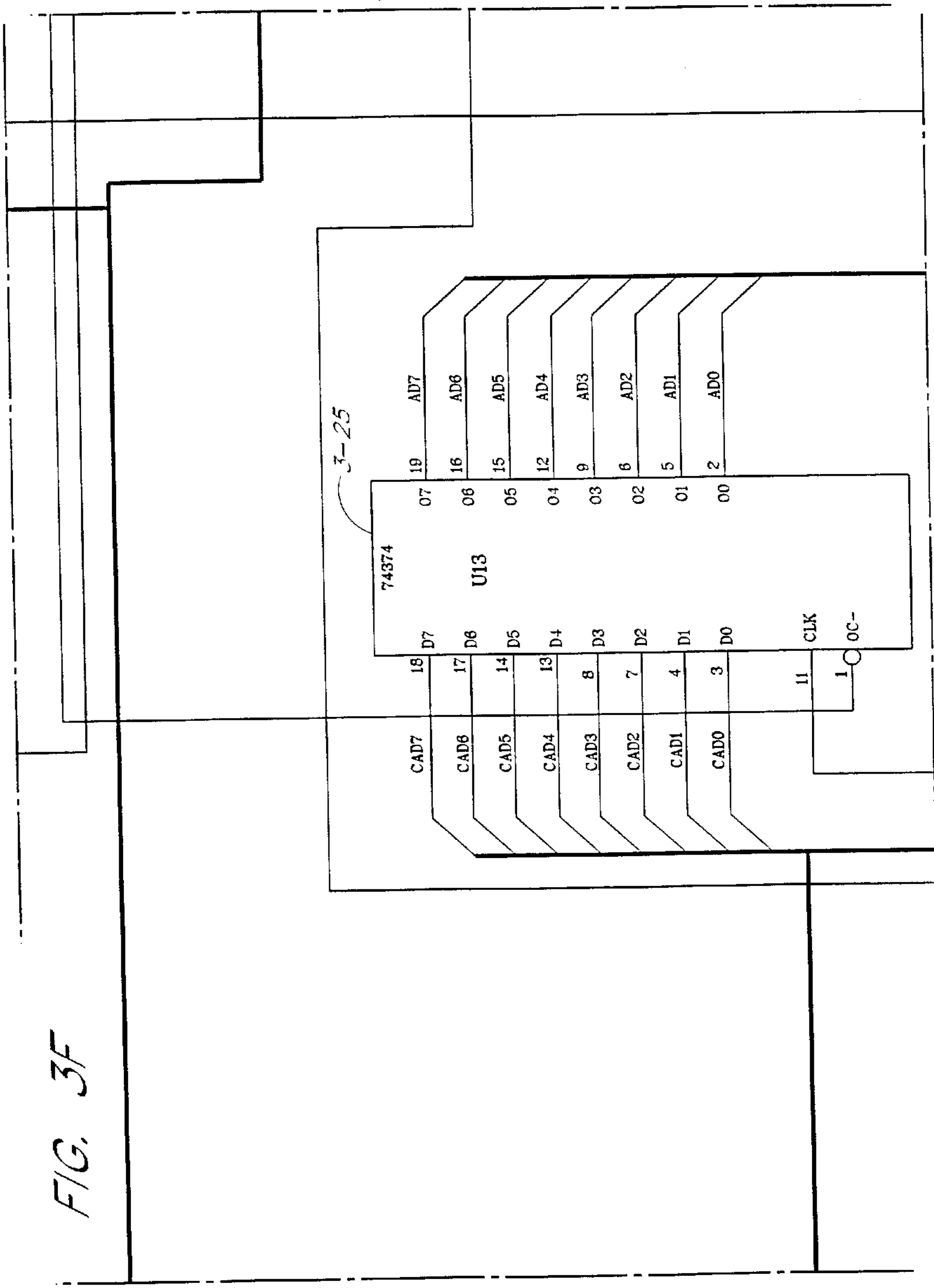

3-25
74374
U13
O7 O6 O5 O4 O3 O2 O1 O0
19 16 15 12 9 6 5 2
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
D7 D6 D5 D4 D3 D2 D1 D0 CLK OC-
18 17 14 13 8 7 4 3 11 1
CAD7 CAD6 CAD5 CAD4 CAD3 CAD2 CAD1 CAD0

FIG. 3F

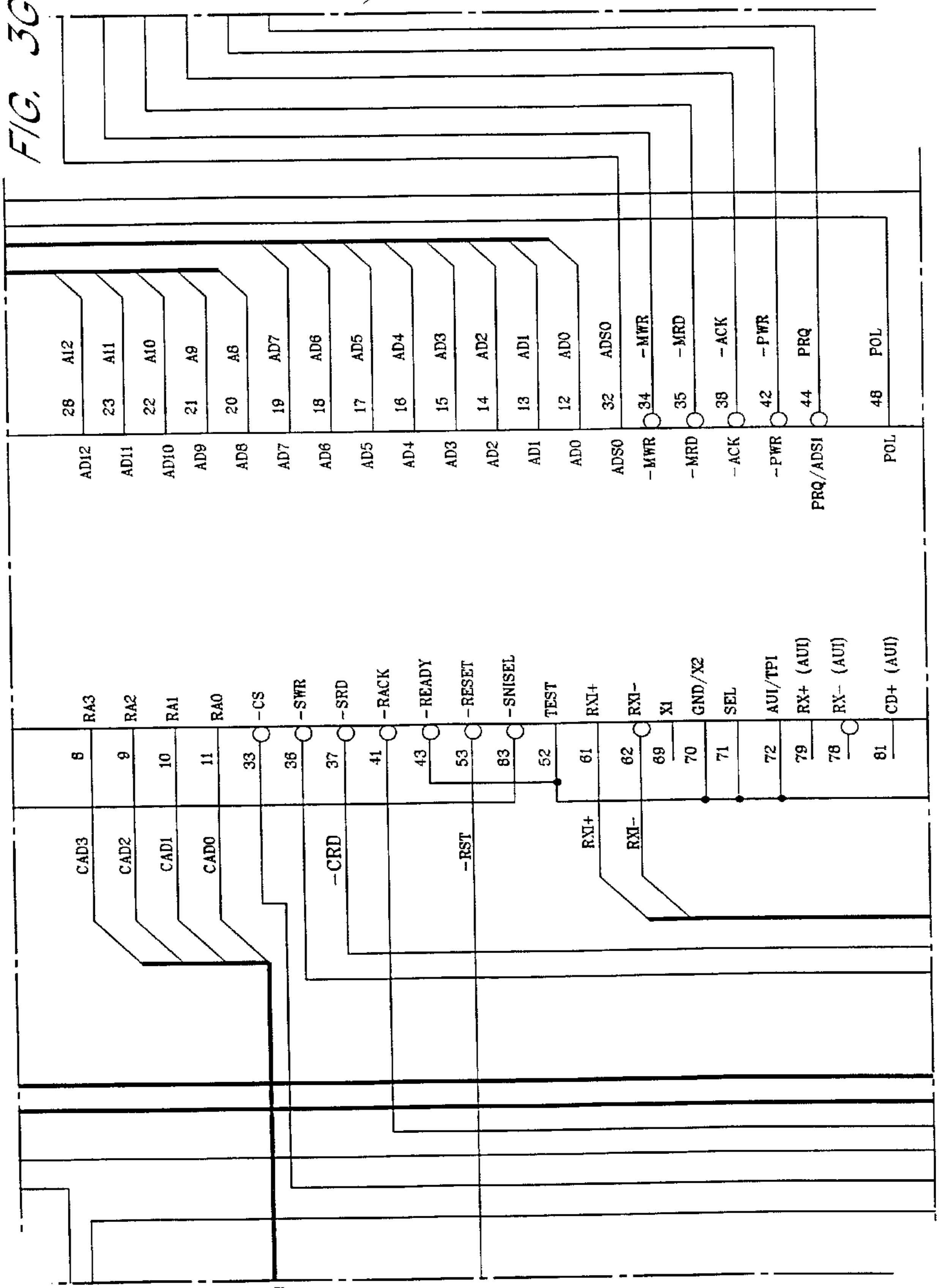

A12
A11
A10
A9
A8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
ADS0
-MWR
-MRD
-ACK
-PWR
PRQ
POL
28
23
22
21
20
19
18
17
16
15
14
13
12
32
34
35
38
42
44
48
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
ADS0
-MWR
-MRD
-ACK
-PWR
PRQ/ADS1
POL
RA3
RA2
RA1
RA0
-CS
-SWR
-SRD
-RACK
-READY
-RESET
-SNISEL
TEST
RXI+
RXI-
X1
GND/X2
SEL
AUI/TPI
RX+ (AUI)
RX- (AUI)
CD+ (AUI)
8
9
10
11
33
36
37
41
43
53
83
52
61
62
69
70
71
72
79
78
81
CAD3
CAD2
CAD1
CAD0
-CRD
-RST
RXI+
RXI-

FIG. 3G

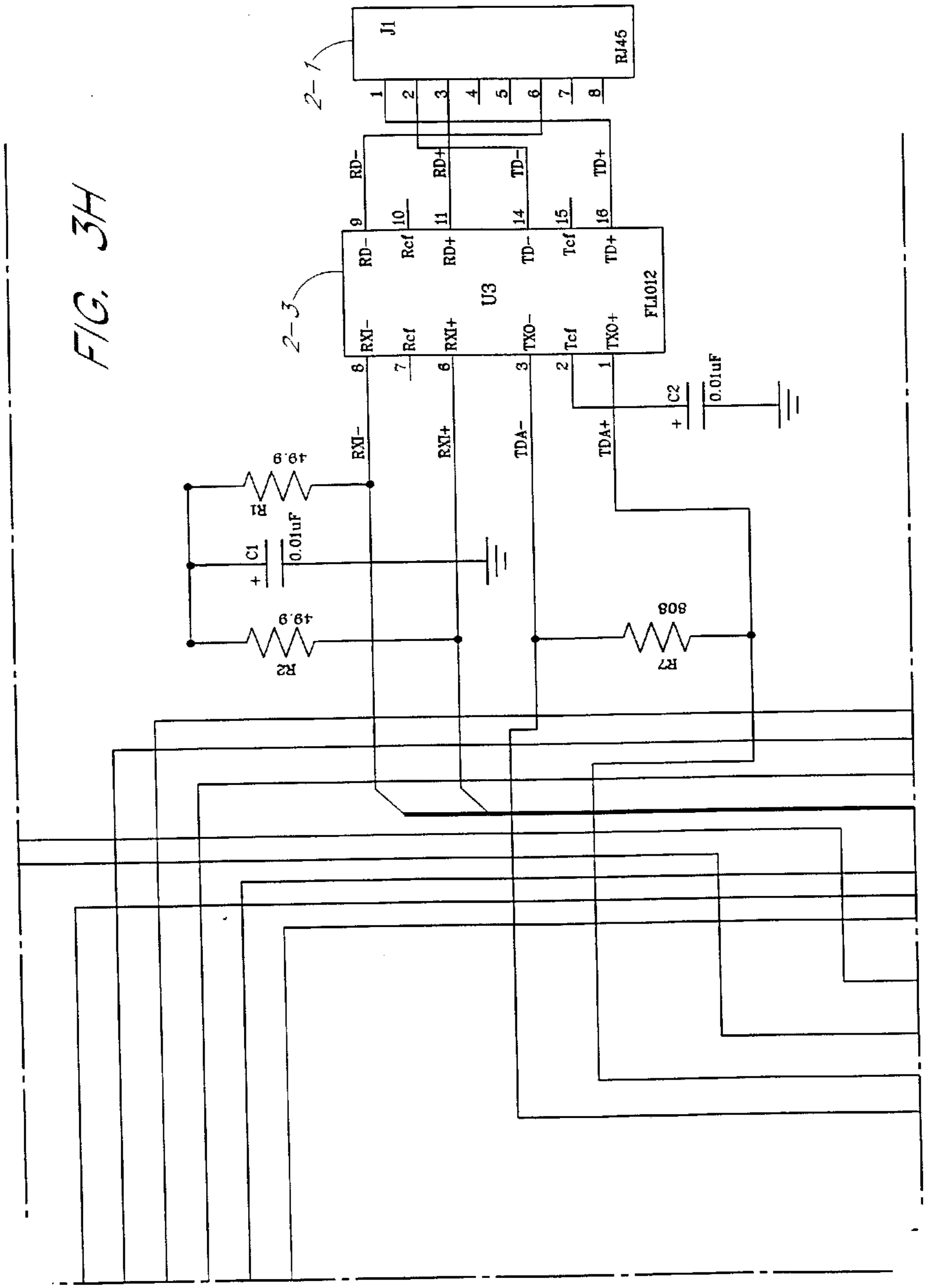

J1
RJ45
2-1
1 2 3 4 5 6 7 8
RD-
RD+
TD-
TD+
9 10 11 14 15 16
RD- Rcf RD+ TD- Tcf TD+
U3
FL1012
2-3
RXI- Rcf RXI+ TXO- Tcf TXO+
8 7 6 3 2 1
C2
0.01uF
RXI-
RXI+
TDA-
TDA+
R1
49.9
C1
0.01uF
R2
49.9
R7
808

FIG. 3H

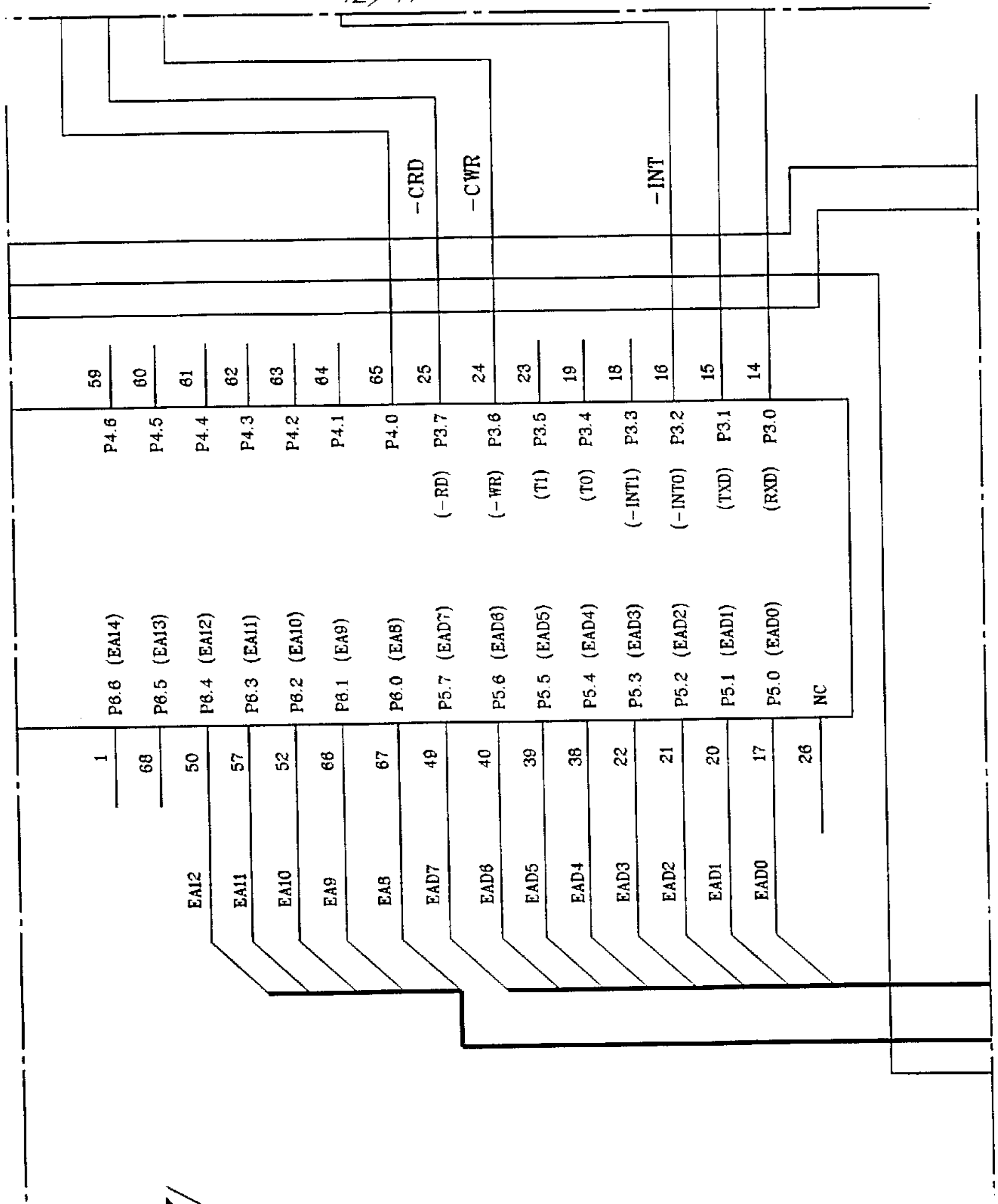

-CRD
-CWR
-INT
59 P4.6
60 P4.5
61 P4.4
62 P4.3
63 P4.2
64 P4.1
65 P4.0
25 P3.7 (-RD)
24 P3.6 (-WR)
23 P3.5 (T1)
19 P3.4 (T0)
18 P3.3 (-INT1)
16 P3.2 (-INT0)
15 P3.1 (TXD)
14 P3.0 (RXD)
1 P6.6 (EA14)
68 P6.5 (EA13)
50 P6.4 (EA12)
57 P6.3 (EA11)
52 P6.2 (EA10)
66 P6.1 (EA9)
67 P6.0 (EA8)
49 P5.7 (EAD7)
40 P5.6 (EAD6)
39 P5.5 (EAD5)
38 P5.4 (EAD4)
22 P5.3 (EAD3)
21 P5.2 (EAD2)
20 P5.1 (EAD1)
17 P5.0 (EAD0)
26 NC
EA12
EA11
EA10
EA9
EA8
EAD7
EAD6
EAD5
EAD4
EAD3
EAD2
EAD1
EAD0

FIG. 3I

13/47

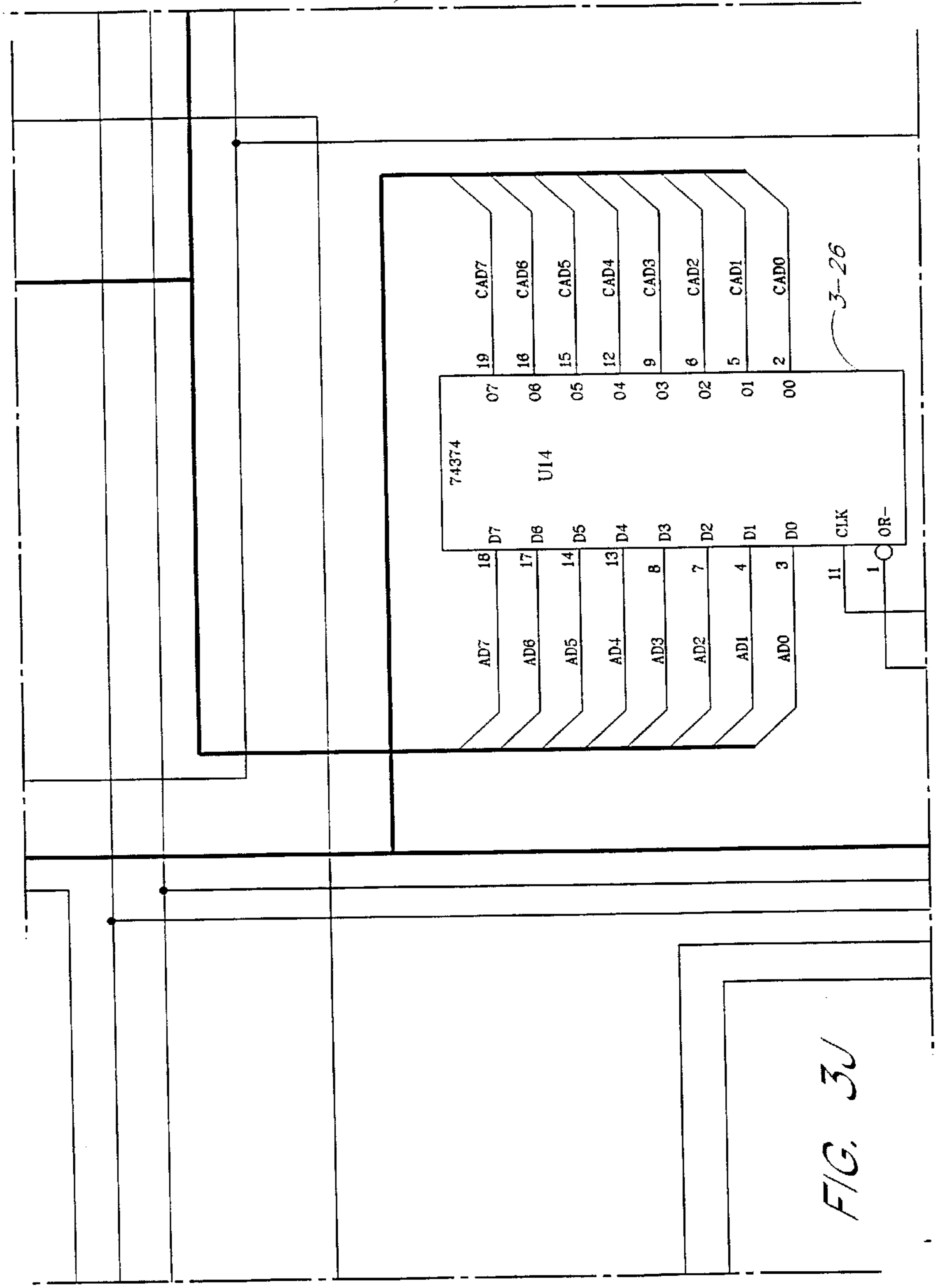

74374
U14
3-26
CAD7
CAD6
CAD5
CAD4
CAD3
CAD2
CAD1
CAD0
O7
O6
O5
O4
O3
O2
O1
O0
D7
D6
D5
D4
D3
D2
D1
D0
CLK
OR-
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
19
16
15
12
9
6
5
2
18
17
14
13
8
7
4
3
11
1

FIG. 3J

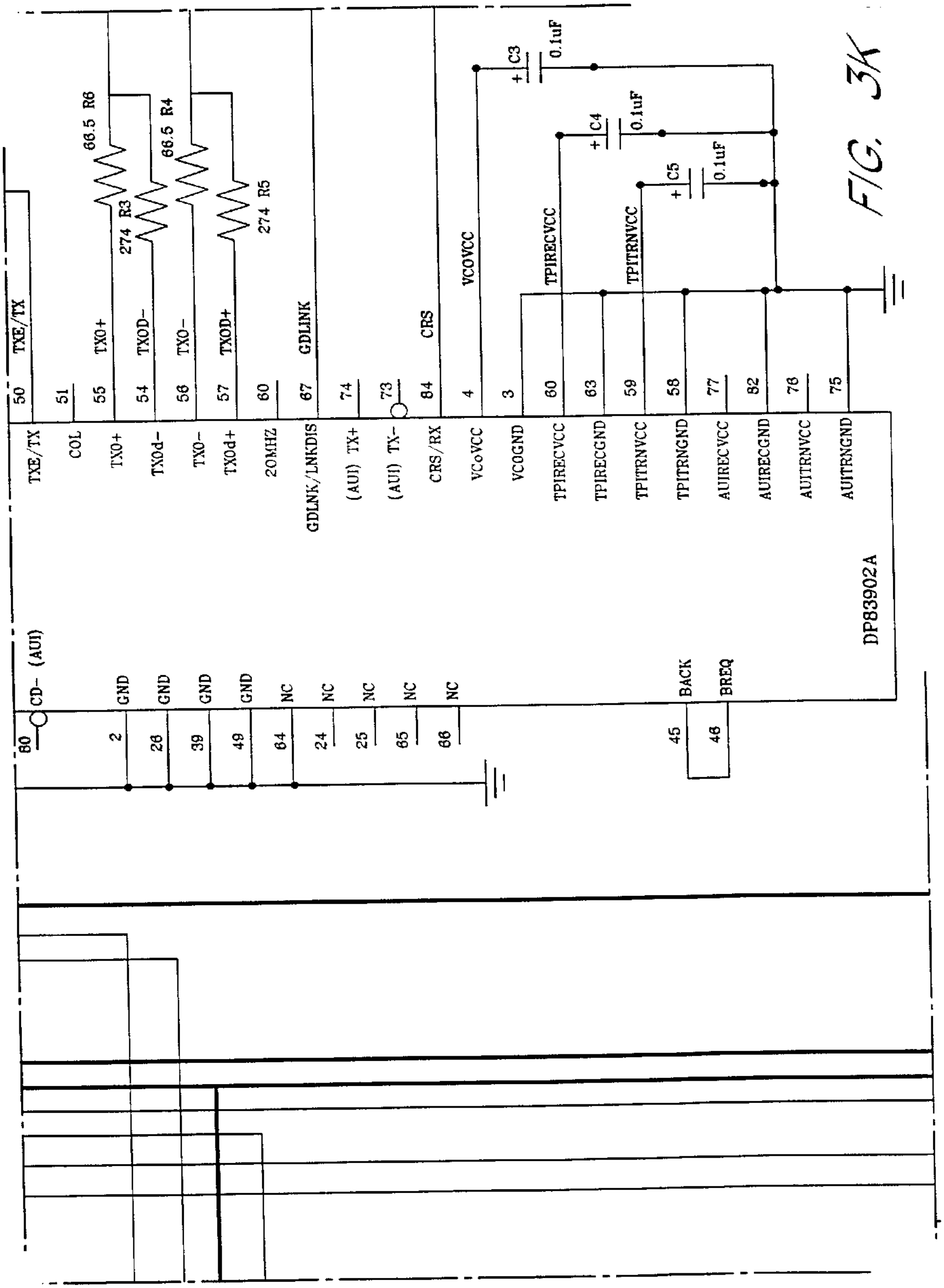
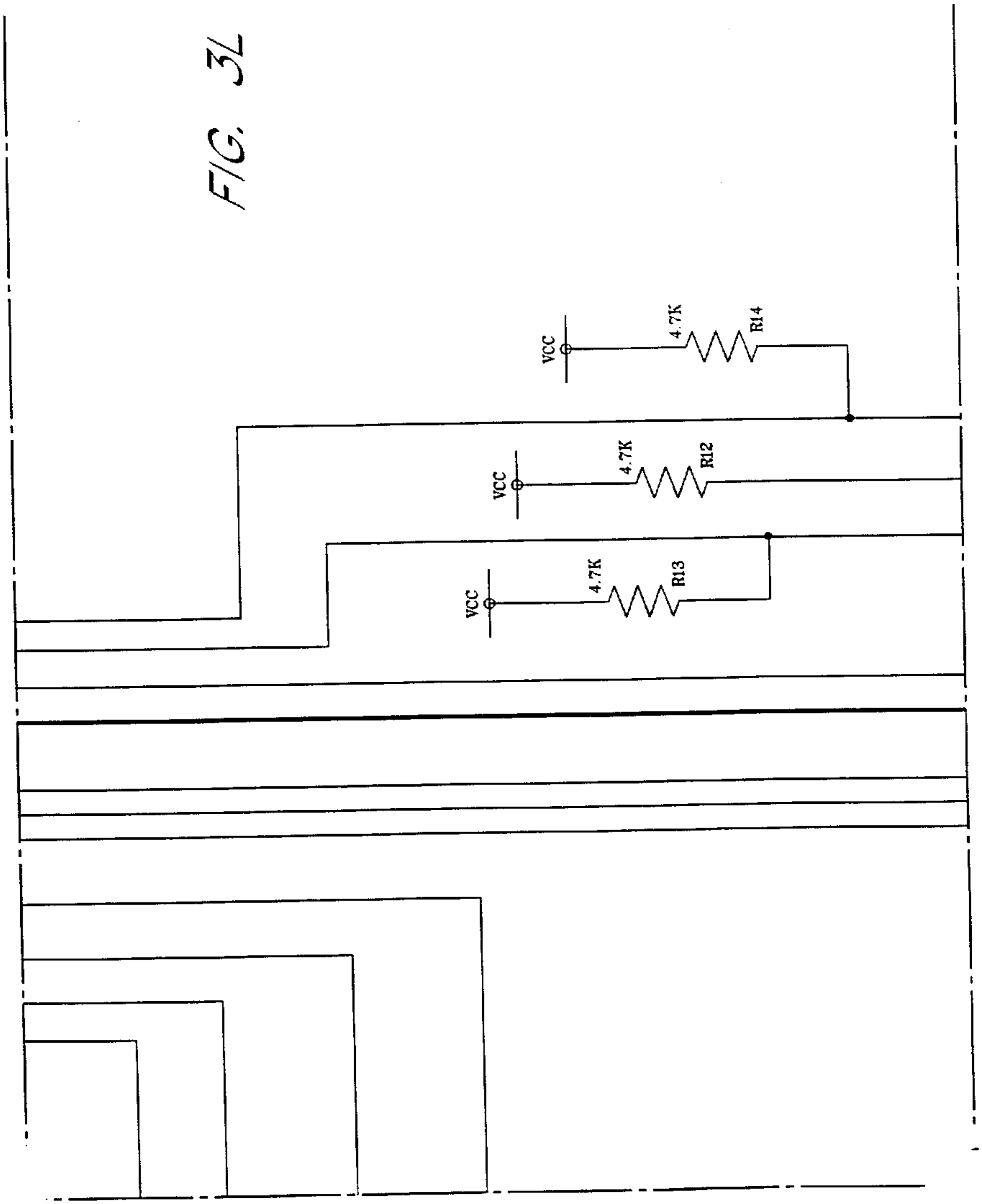

TXE/TX
TX0+
TX0D-
TX0-
TX0D+
GDLINK
CRS
VCOVCC
TPIRECVCC
TPITRNVCC
66.5 R6
274 R3
66.5 R4
274 R5
C3
0.1uF
C4
0.1uF
C5
0.1uF
50
51
55
54
56
57
60
67
74
73
84
4
3
80
83
59
58
77
82
76
75
TXE/TX
COL
TX0+
TX0d-
TX0-
TX0d+
20MHZ
GDLNK/LNKDIS
(AUI) TX+
(AUI) TX-
CRS/RX
VCoVCC
VCOGND
TPIRECVCC
TPIRECGND
TPITRNVCC
TPITRNGND
AUIRECVCC
AUIRECGND
AUITRNVCC
AUITRNGND
DP83902A
CD- (AUI)
GND
GND
GND
GND
NC
NC
NC
NC
NC
BACK
BREQ
60
2
26
39
49
64
24
25
65
66
45
46

FIG. 3K

FIG. 3L



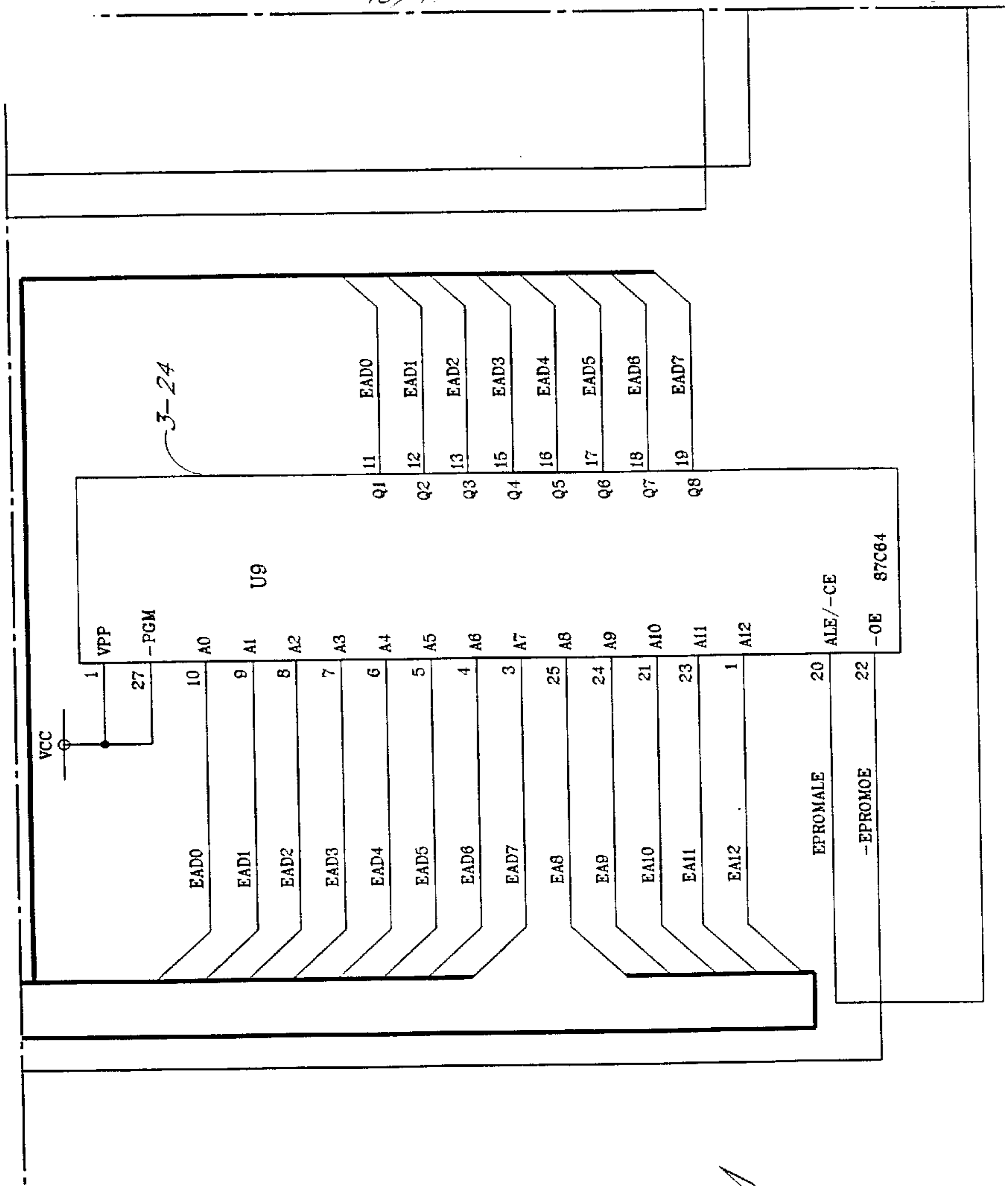

3-24
U9
87C64
VCC
VPP
-PGM
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
ALE/-CE
-OE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
1
27
10
9
8
7
6
5
4
3
25
24
21
23
1
20
22
11
12
13
15
16
17
18
19
EAD0
EAD1
EAD2
EAD3
EAD4
EAD5
EAD6
EAD7
EA8
EA9
EA10
EA11
EA12
EPROMALE
-EPROMOE

FIG. 3M

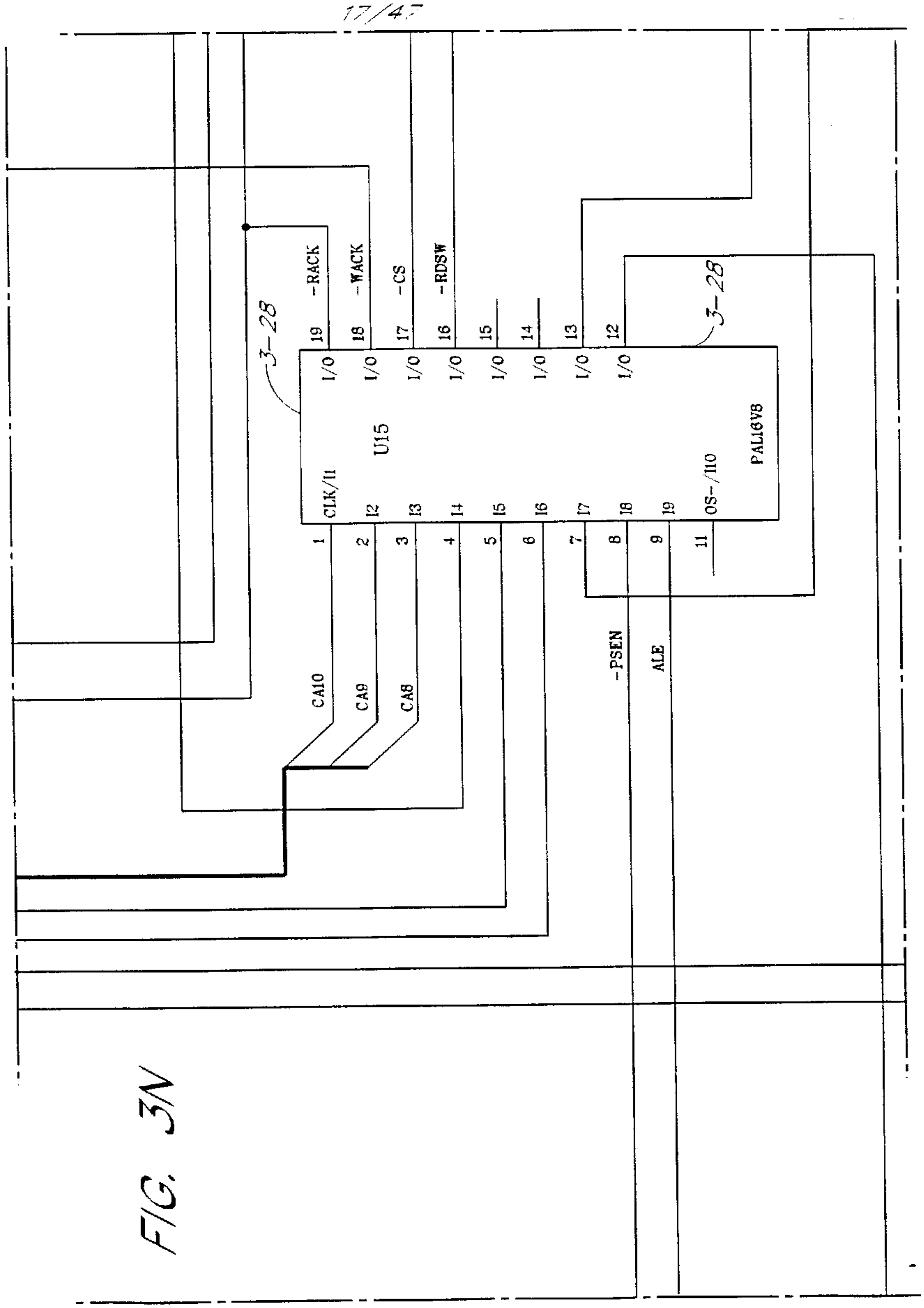

-RACK
-WACK
-CS
-RDSW
3-28
3-28
19
18
17
16
15
14
13
12
I/O
U15
PAL16V8
CLK/I1
I2
I3
I4
I5
I6
I7
I8
I9
OS-/I10
1
2
3
4
5
6
7
8
9
11
CA10
CA9
CA8
-PSEN
ALE

FIG. 3N

18/47

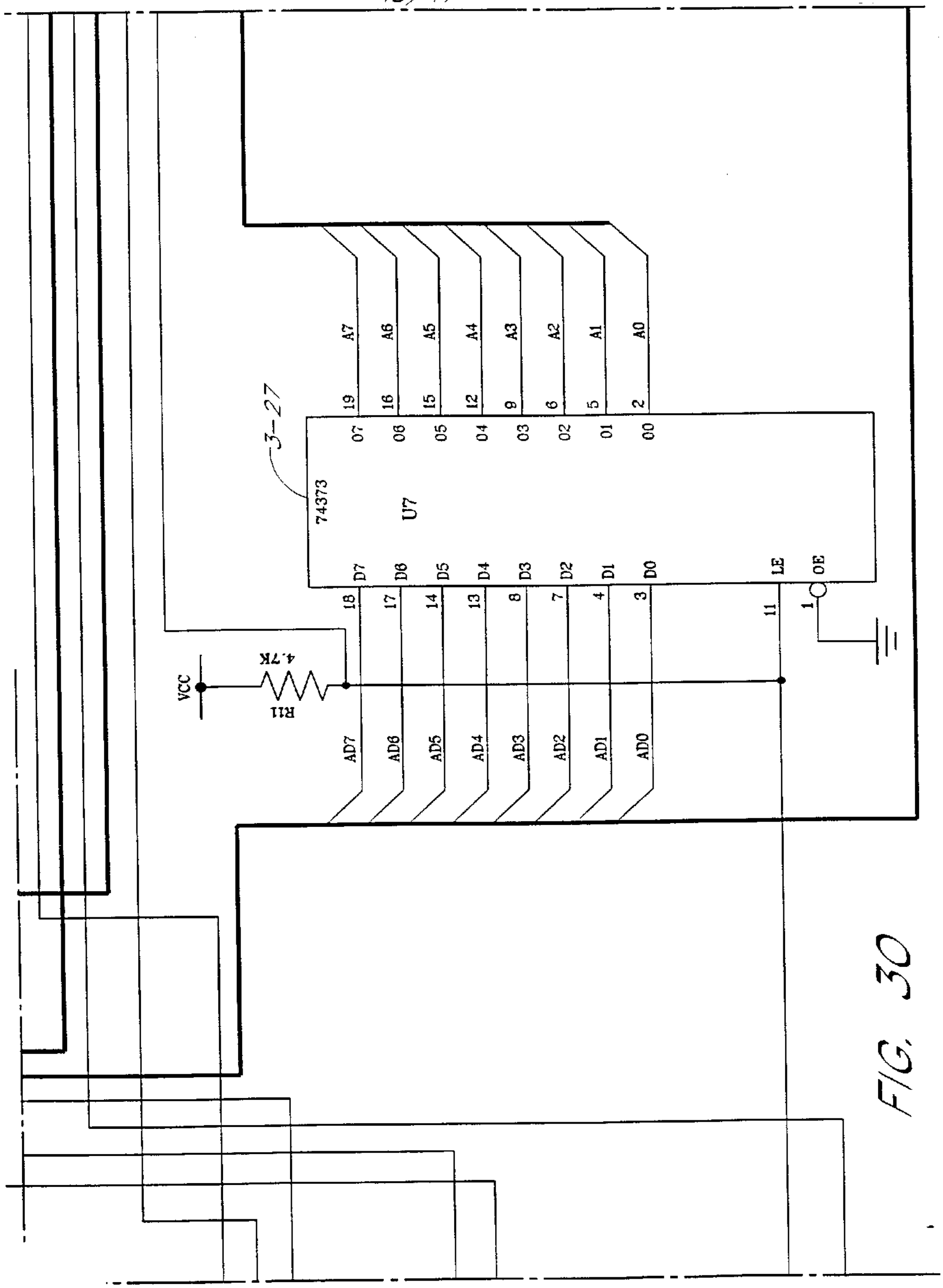

3-27
74373
U7
07
06
05
04
03
02
01
00
19
16
15
12
9
6
5
2
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
LE
OE
18
17
14
13
8
7
4
3
11
1
VCC
4.7K
R11
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0

FIG. 30

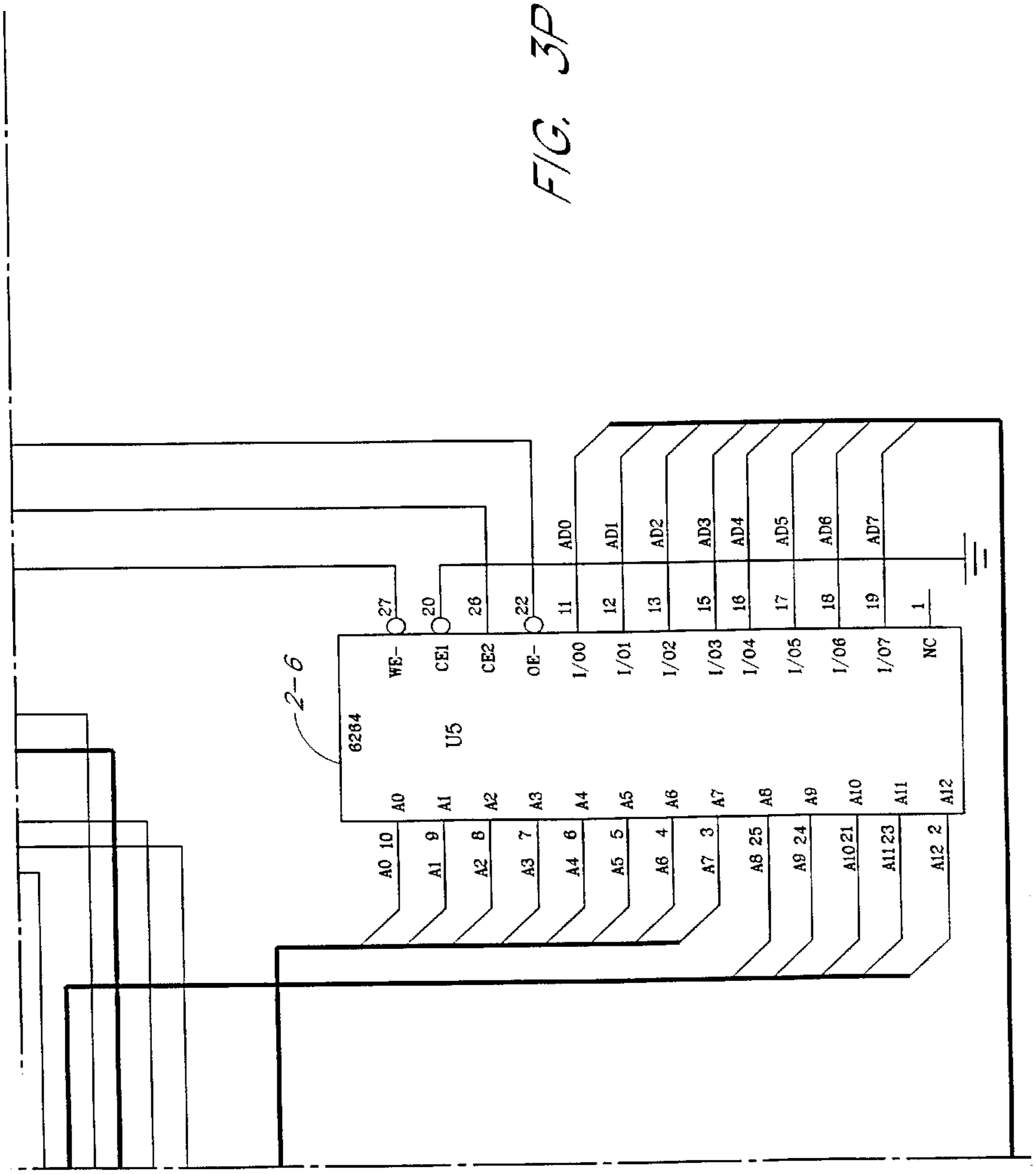

U5
6264
2-6
WE-
CE1
CE2
OE-
I/00
I/01
I/02
I/03
I/04
I/05
I/06
I/07
NC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
A0 10
A1 9
A2 8
A3 7
A4 6
A5 5
A6 4
A7 3
A8 25
A9 24
A10 21
A11 23
A12 2
27
20
26
22
11
12
13
15
16
17
18
19
1

FIG. 3P

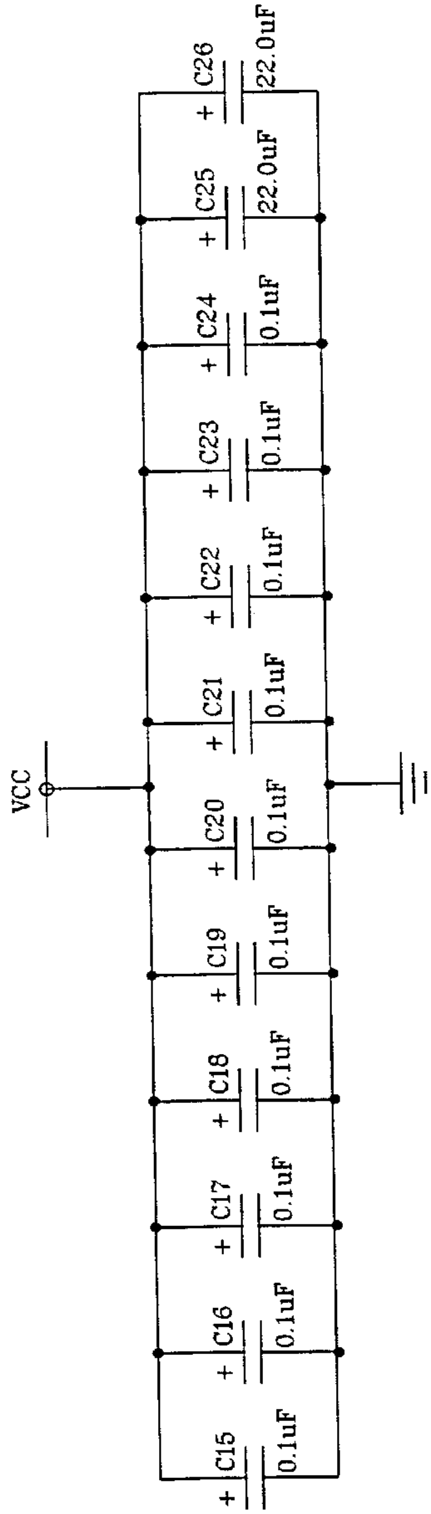
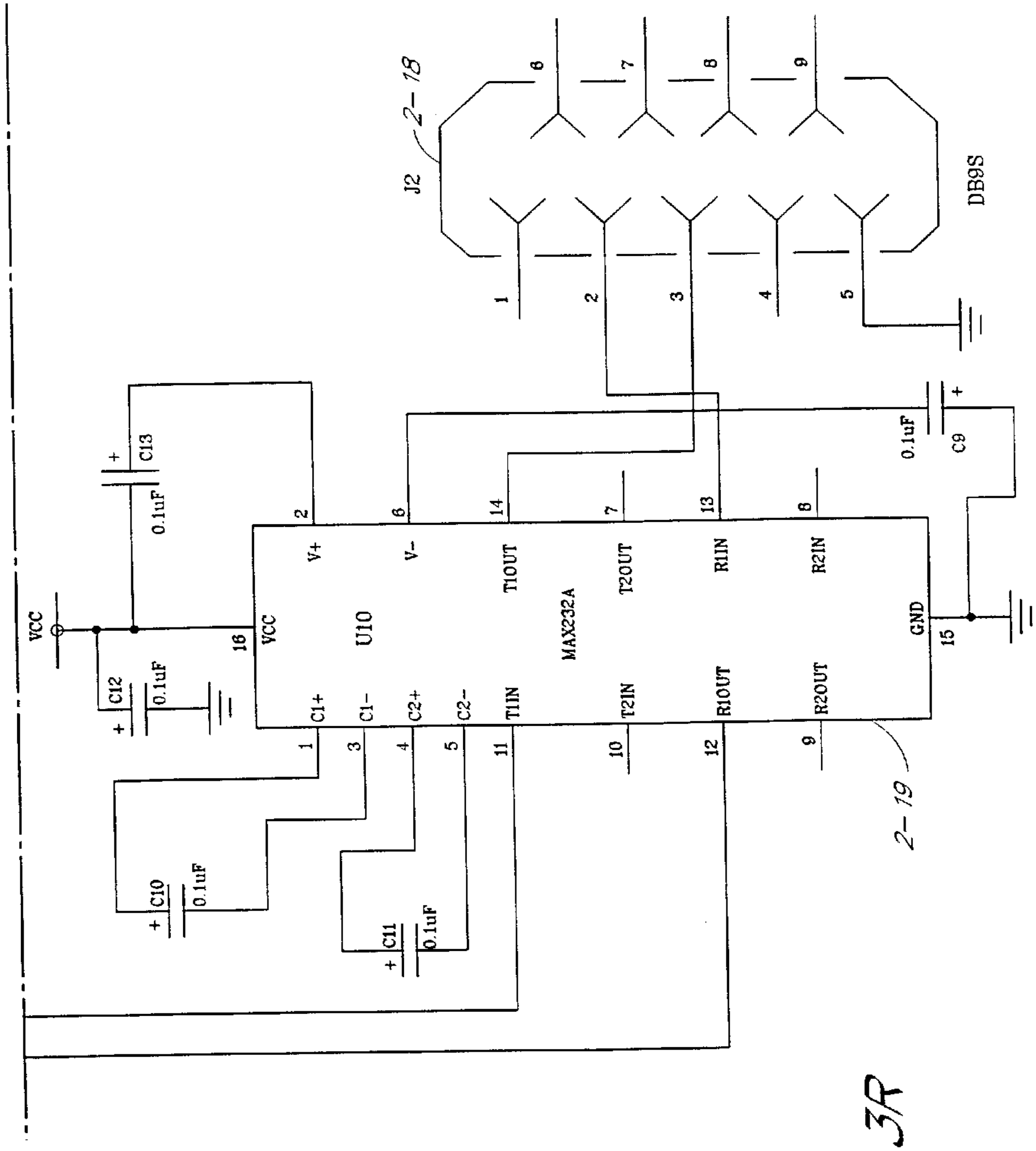

VCC
C15
0.1uF
C16
0.1uF
C17
0.1uF
C18
0.1uF
C19
0.1uF
C20
0.1uF
C21
0.1uF
C22
0.1uF
C23
0.1uF
C24
0.1uF
C25
22.0uF
C26
22.0uF

FIG. 3Q

21/47



J2
2-18
DB9S
1
2
3
4
5
6
7
8
9
VCC
C12
0.1uF
C13
0.1uF
C10
0.1uF
C11
0.1uF
C9
0.1uF
U10
MAX232A
V+
V-
T1OUT
T2OUT
R1IN
R2IN
VCC
GND
C1+
C1-
C2+
C2-
T1IN
T2IN
R1OUT
R2OUT
16
15
14
13
12
11
10
2-19

FIG. 3R

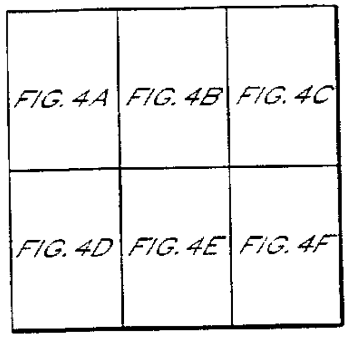


FIG. 4A
FIG. 4B
FIG. 4C
FIG. 4D
FIG. 4E
FIG. 4F

FIG. 4

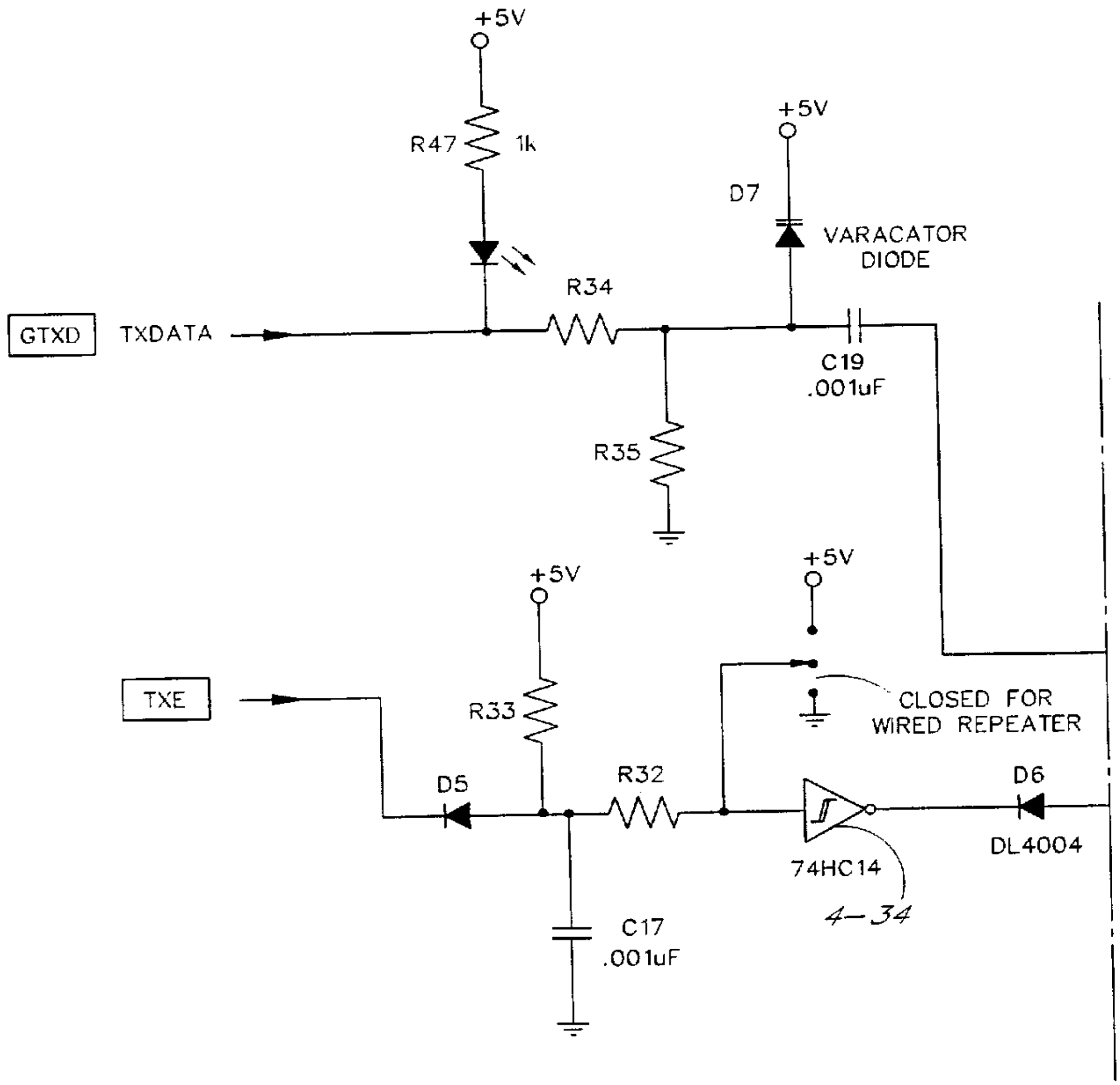

+5V
R47
1k
+5V
D7
VARACATOR DIODE
R34
GTXD
TXDATA
C19
.001uF
R35
+5V
+5V
TXE
R33
CLOSED FOR WIRED REPEATER
D5
R32
D6
74HC14
DL4004
4–34
C17
.001uF

FIG. 4A

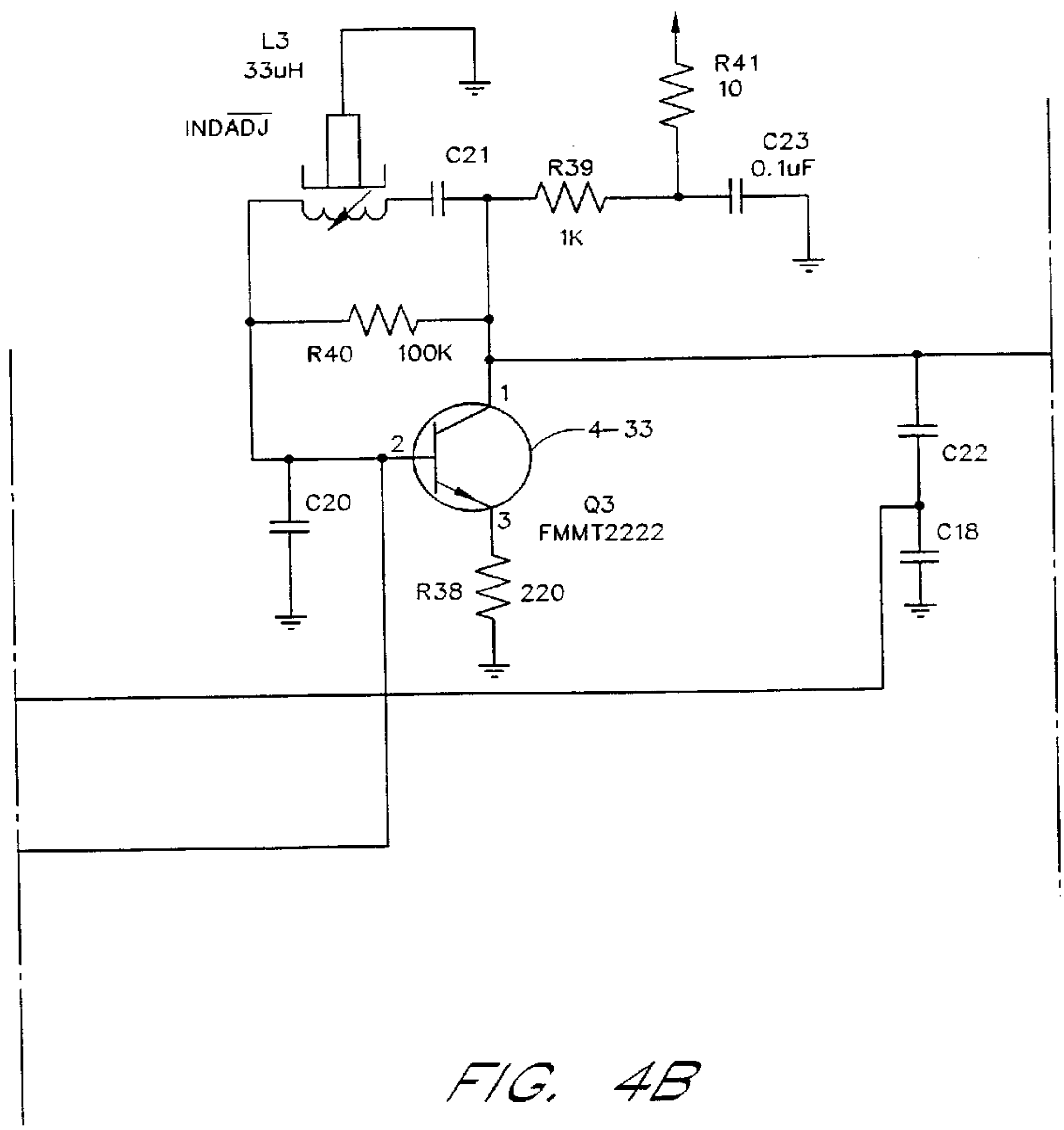

L3
33uH
INDADJ
C21
R39
1K
R41
10
C23
0.1uF
R40
100K
1
2
3
4-33
Q3
FMMT2222
C20
R38
220
C22
C18

FIG. 4B

FIG. 4C

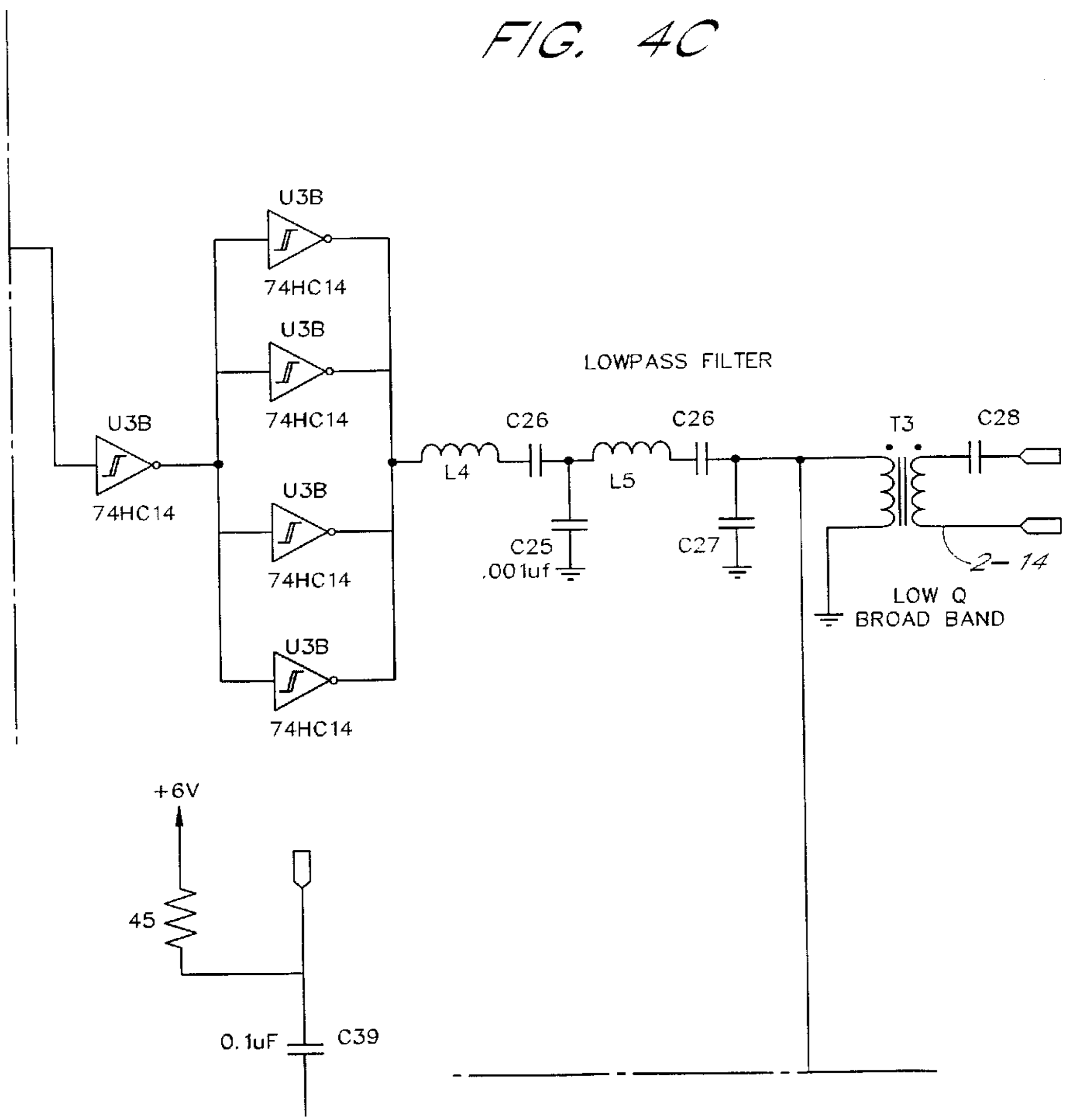
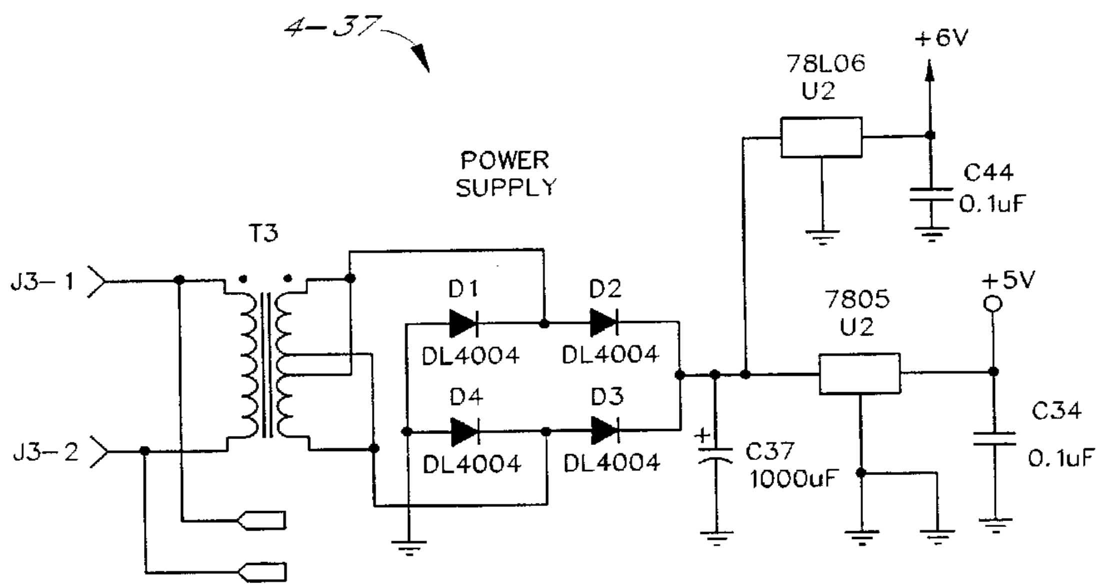

U3B
74HC14
U3B
74HC14
U3B
74HC14
U3B
74HC14
U3B
74HC14
LOWPASS FILTER
C26
L4
C26
L5
C25
.001uf
C27
T3
C28
2-14
LOW Q
BROAD BAND
+6V
45
0.1uF
C39

FIG. 4D


4-37
POWER
SUPPLY
T3
J3- 1
J3- 2
D1
DL4004
D2
DL4004
D4
DL4004
D3
DL4004
C37
1000uF
78L06
U2
+6V
C44
0.1uF
7805
U2
+5V
C34
0.1uF

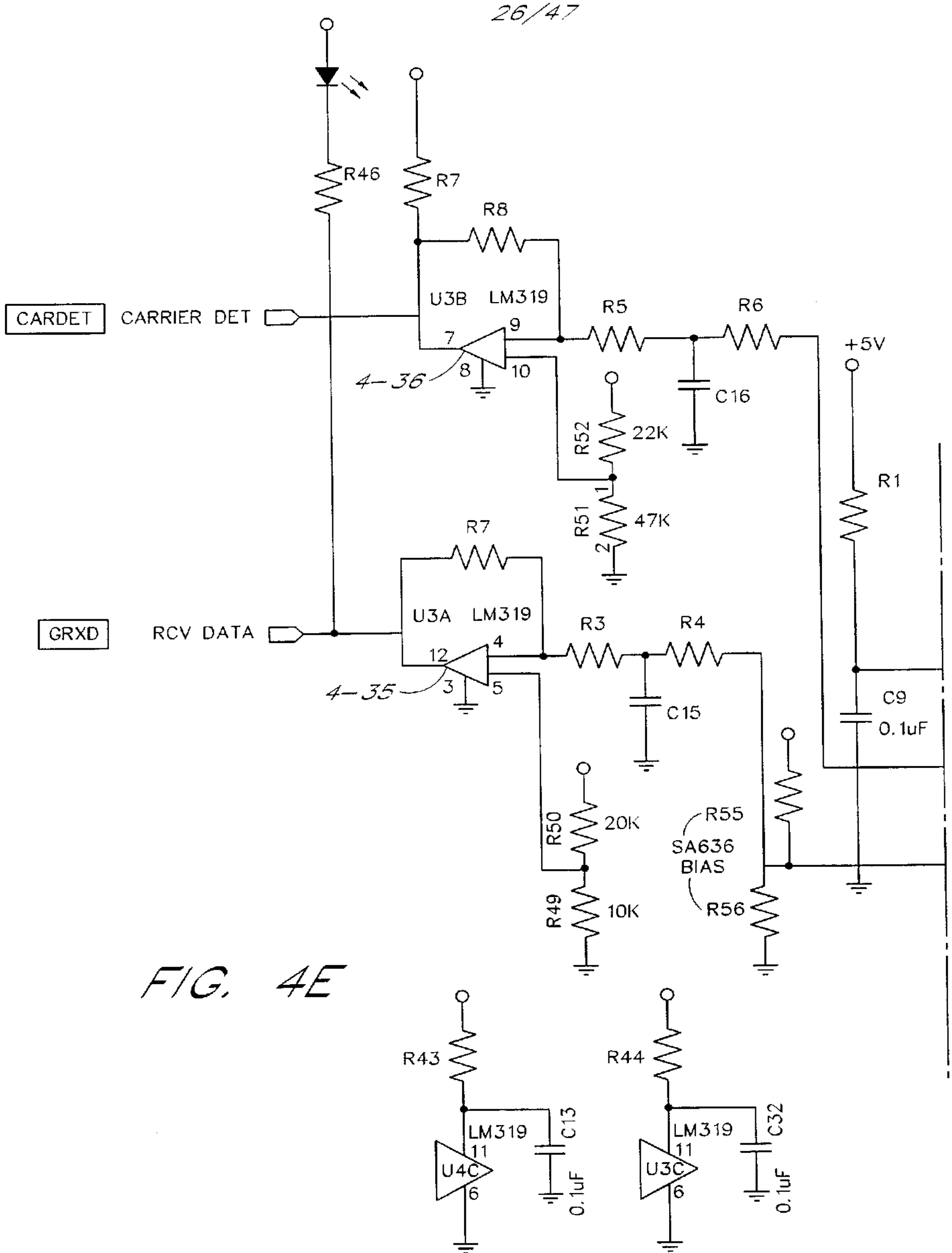
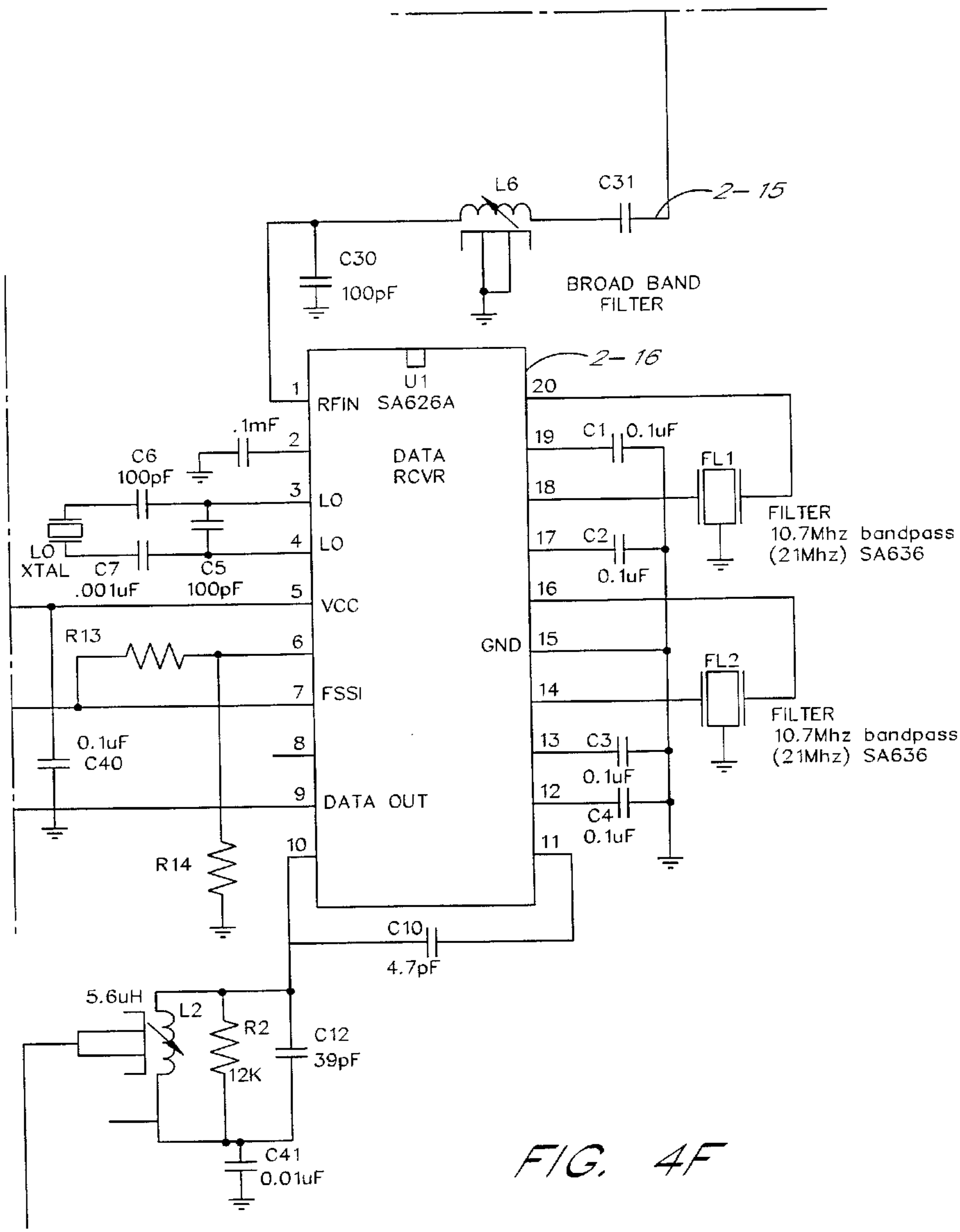
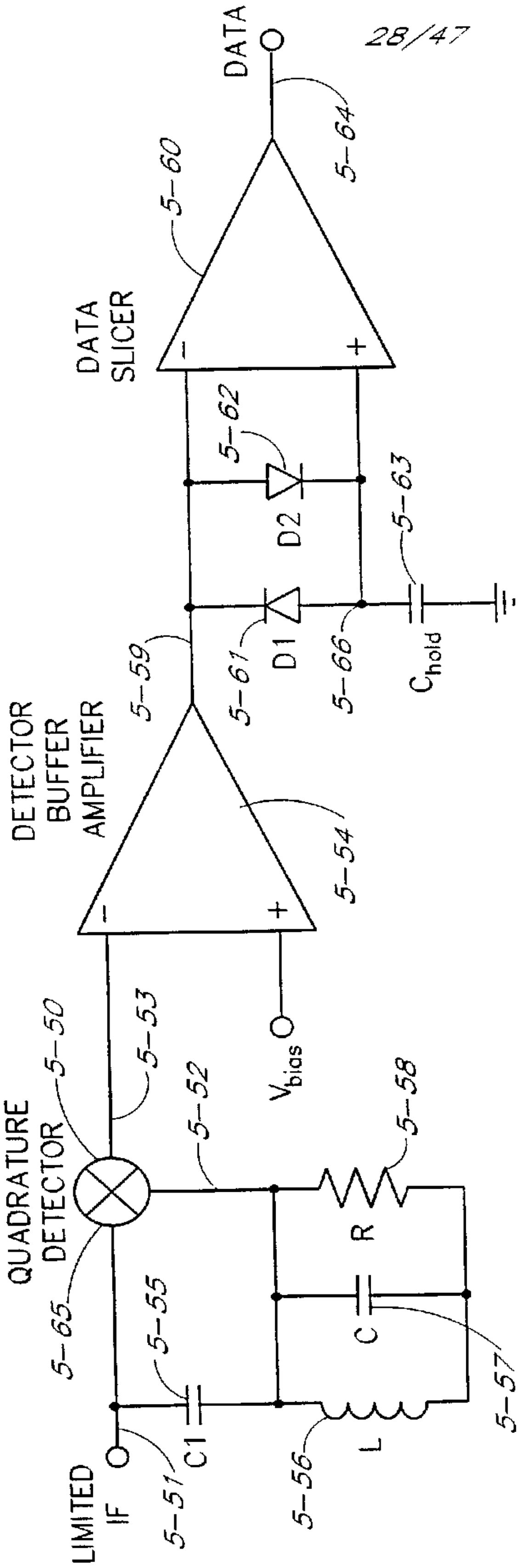

R46
R7
R8
U3B LM319
CARDET
CARRIER DET
R5
R6
+5V
7
9
4-36
8
10
C16
R52
22K
R1
R51
47K
R7
U3A LM319
GRXD
RCV DATA
R3
R4
12
4
4-35
3
5
C15
C9
0.1uF
R55
R50
20K
SA636
BIAS
R49
10K
R56
R43
R44
LM319
11
U4C
6
C13
0.1uF
LM319
11
U3C
6
C32
0.1uF

FIG. 4E



L6
C31
2-15
C30
100pF
BROAD BAND FILTER
2-16
U1
SA626A
DATA RCVR
1 RFIN
.1mF
2
C6
100pF
3 LO
4 LO
LO XTAL
C7
.001uF
C5
100pF
5 VCC
R13
6
7 FSSI
0.1uF
C40
8
9 DATA OUT
10
R14
20
19
C1 0.1uF
FL1
18
17
C2
0.1uF
FILTER
10.7Mhz bandpass
(21Mhz) SA636
16
GND
15
FL2
14
FILTER
10.7Mhz bandpass
(21Mhz) SA636
13
C3
0.1uF
12
C4
0.1uF
11
C10
4.7pF
5.6uH
L2
R2
12K
C12
39pF
C41
0.01uF

FIG. 4F



DATA
5-64
5-60
DATA SLICER
5-62
D2
5-63
5-59
5-61
D1
5-66
C_{hold}
DETECTOR BUFFER AMPLIFIER
5-54
QUADRATURE DETECTOR
5-50
5-53
5-52
V_{bias}
5-58
R
5-65
5-55
C
5-57
LIMITED IF
5-51
C1
5-56
L

FIG. 5

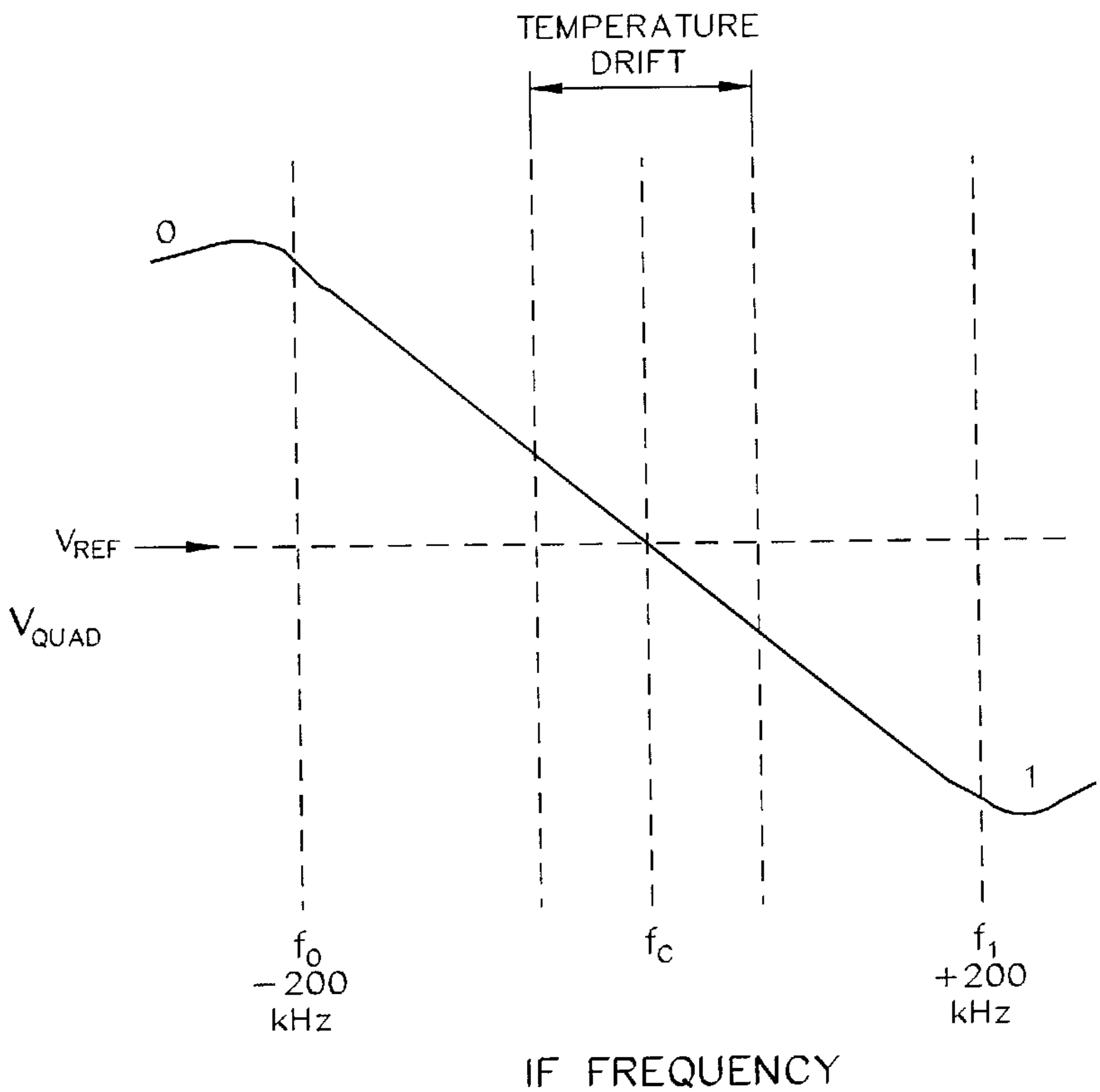
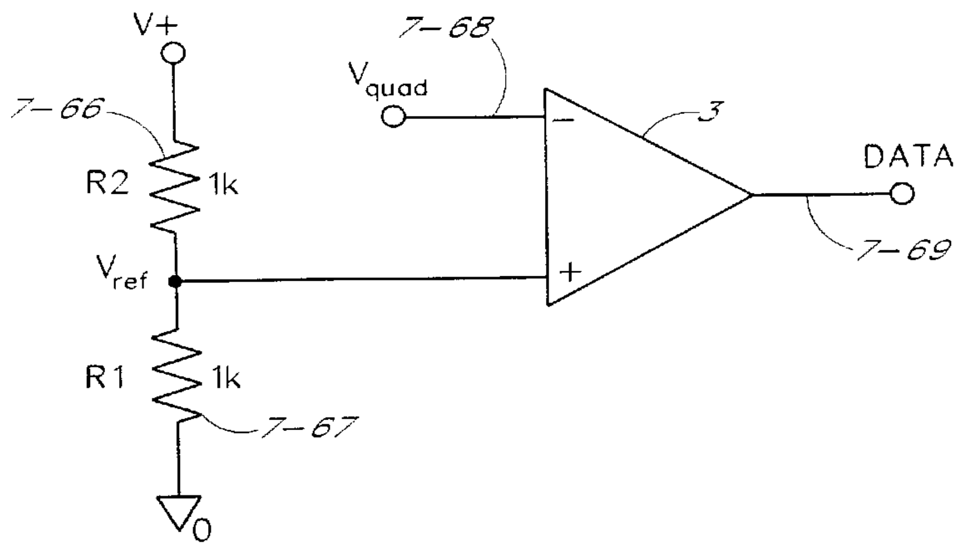

TEMPERATURE DRIFT
0
1
VREF
VQUAD
f0
-200 kHz
fC
f1
+200 kHz
IF FREQUENCY

FIG. 6



DC-coupled FSK data comparator

FIG. 7A

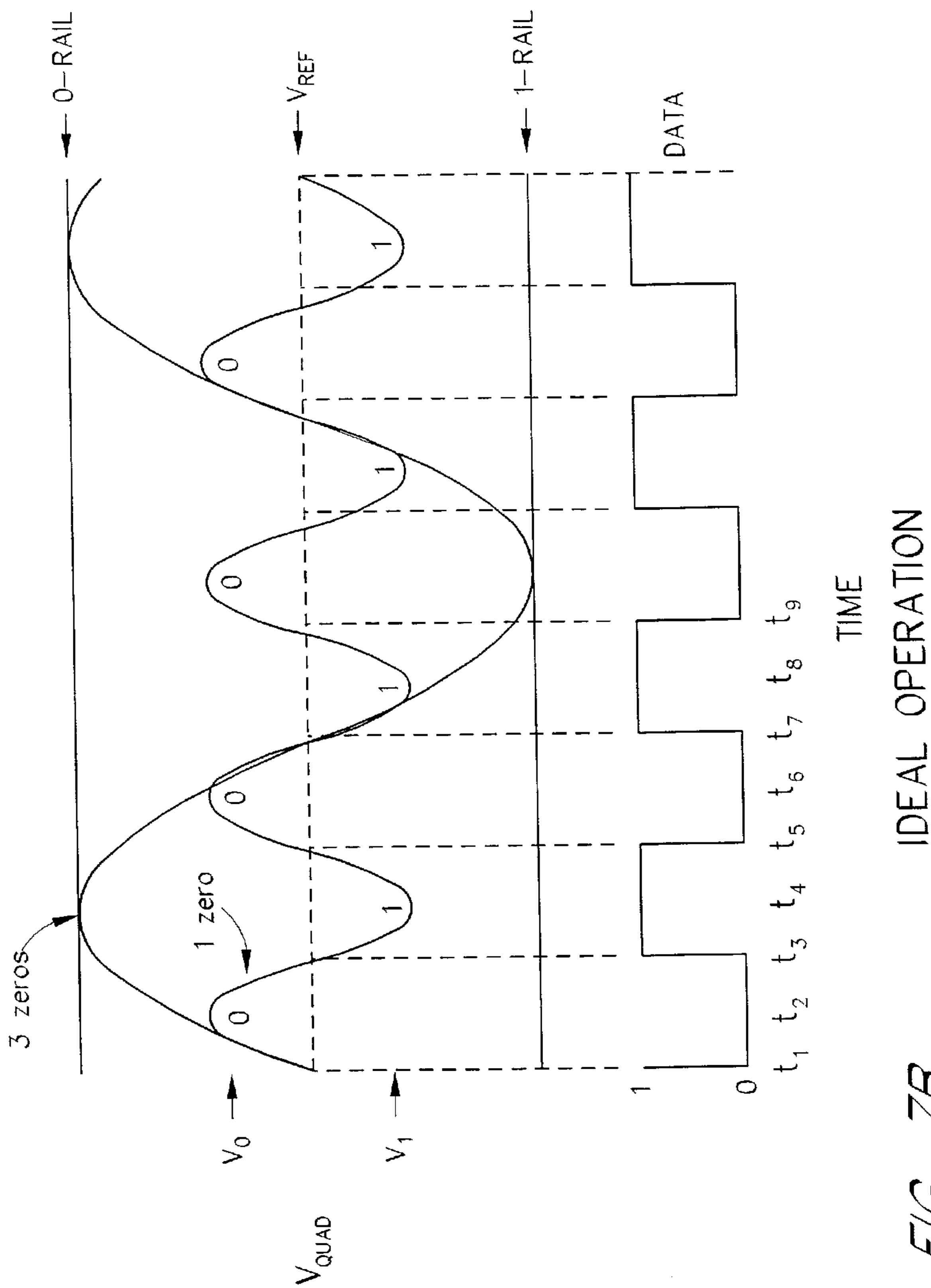
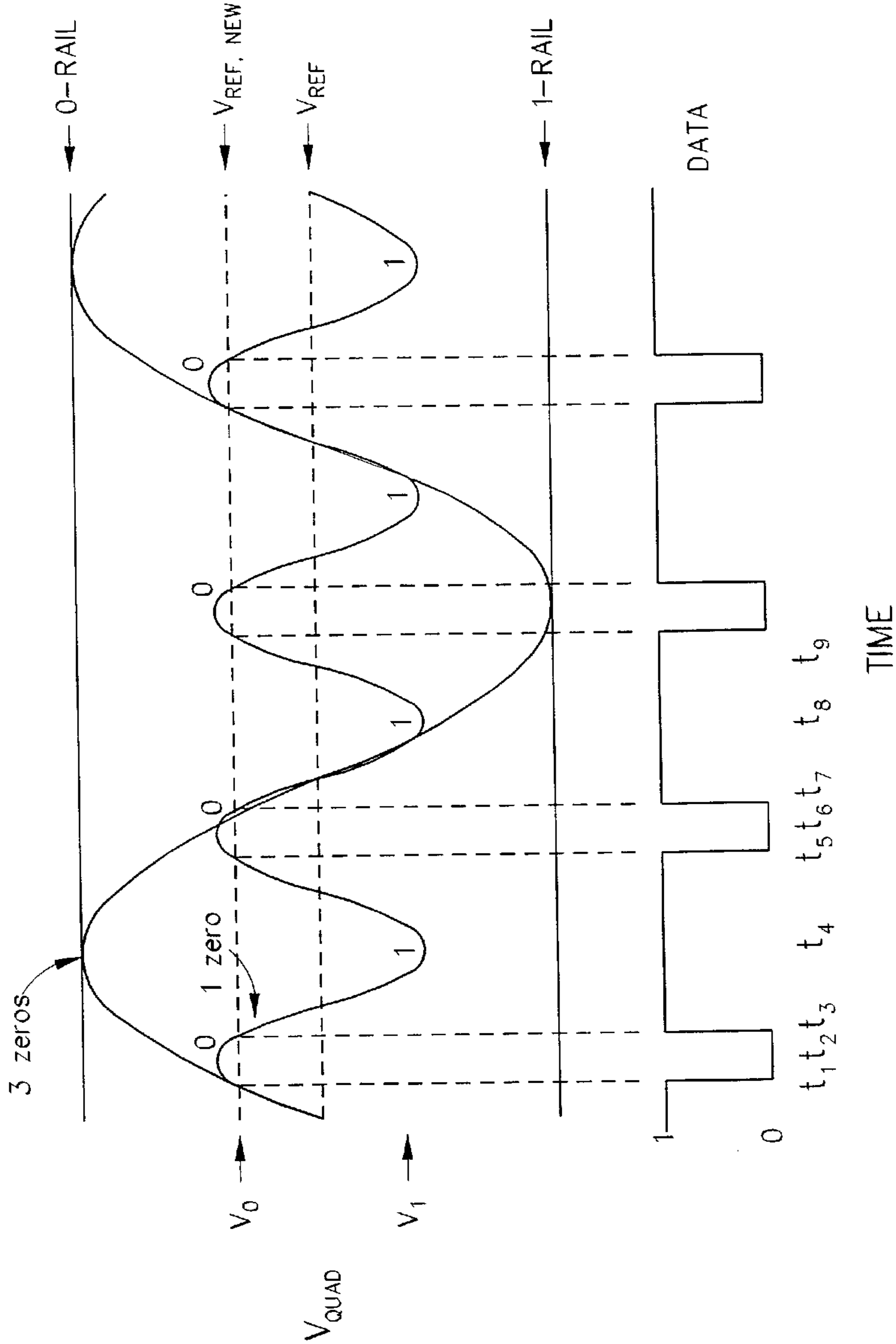
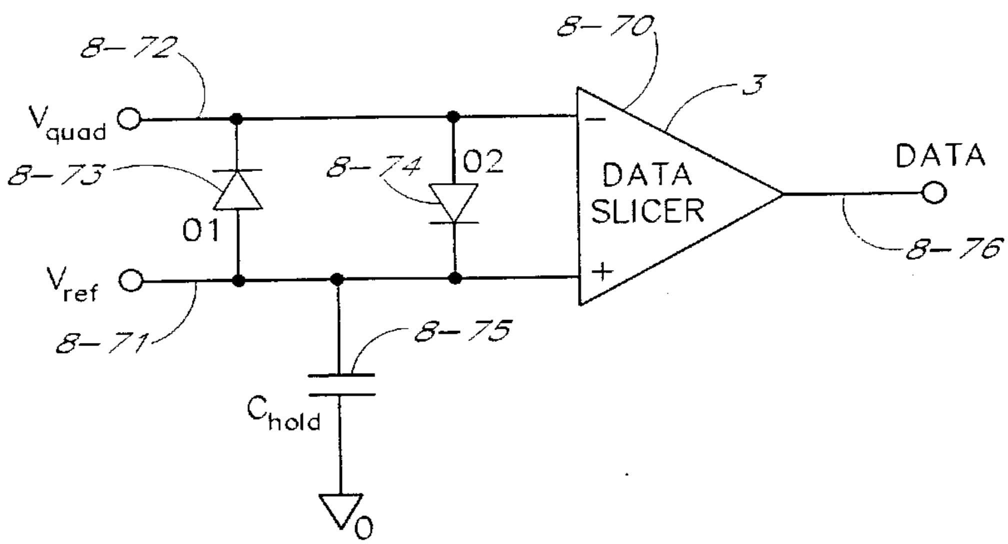

0-RAIL
V_{REF}
1-RAIL
DATA
3 zeros
1 zero
0
1
0
1
0
1
0
1
V_0
V_1
V_{QUAD}
1
0
t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9
TIME
IDEAL OPERATION

FIG. 7B



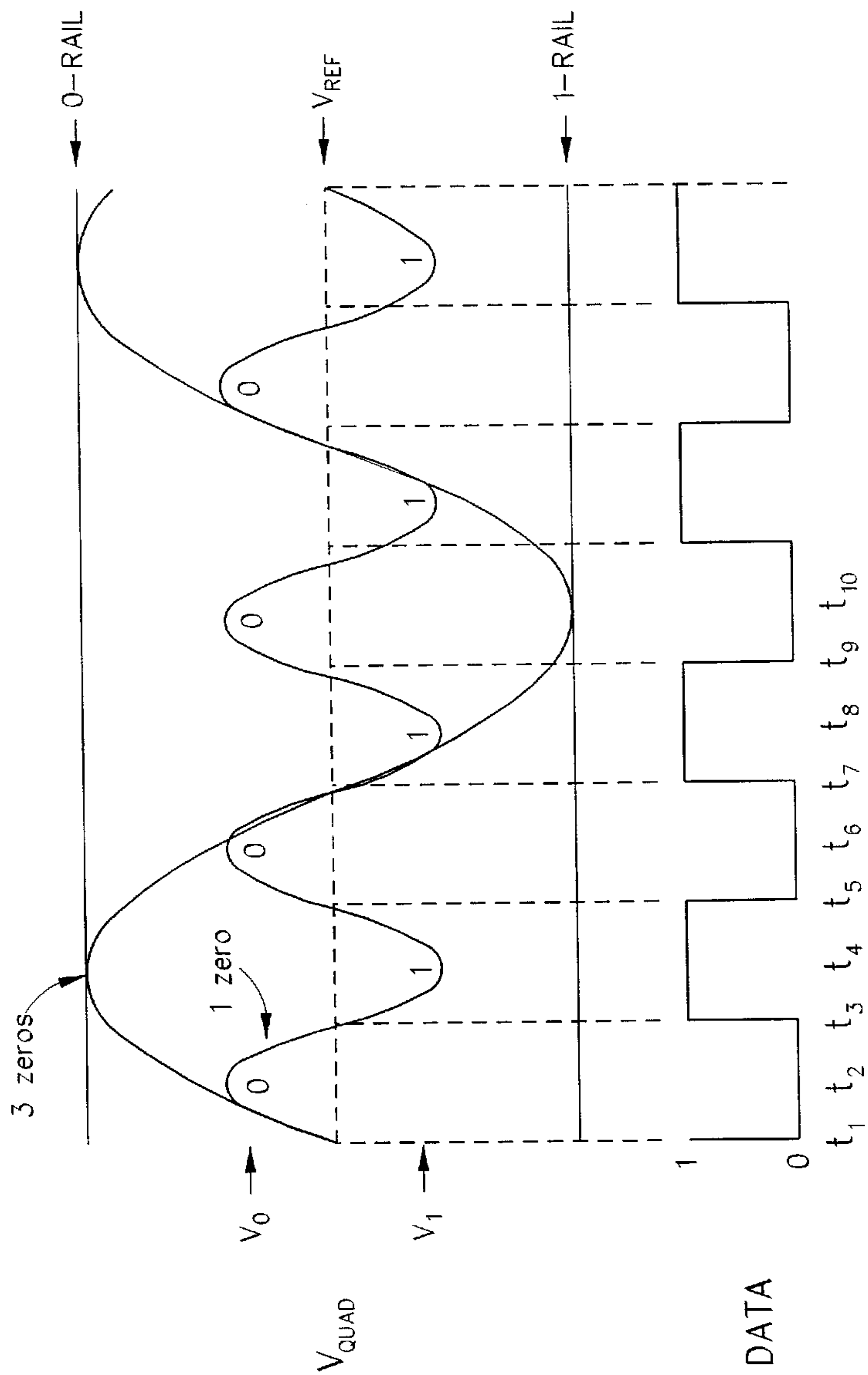
OPERATION WITH SIGNAL DRIFT

FIG. 7C



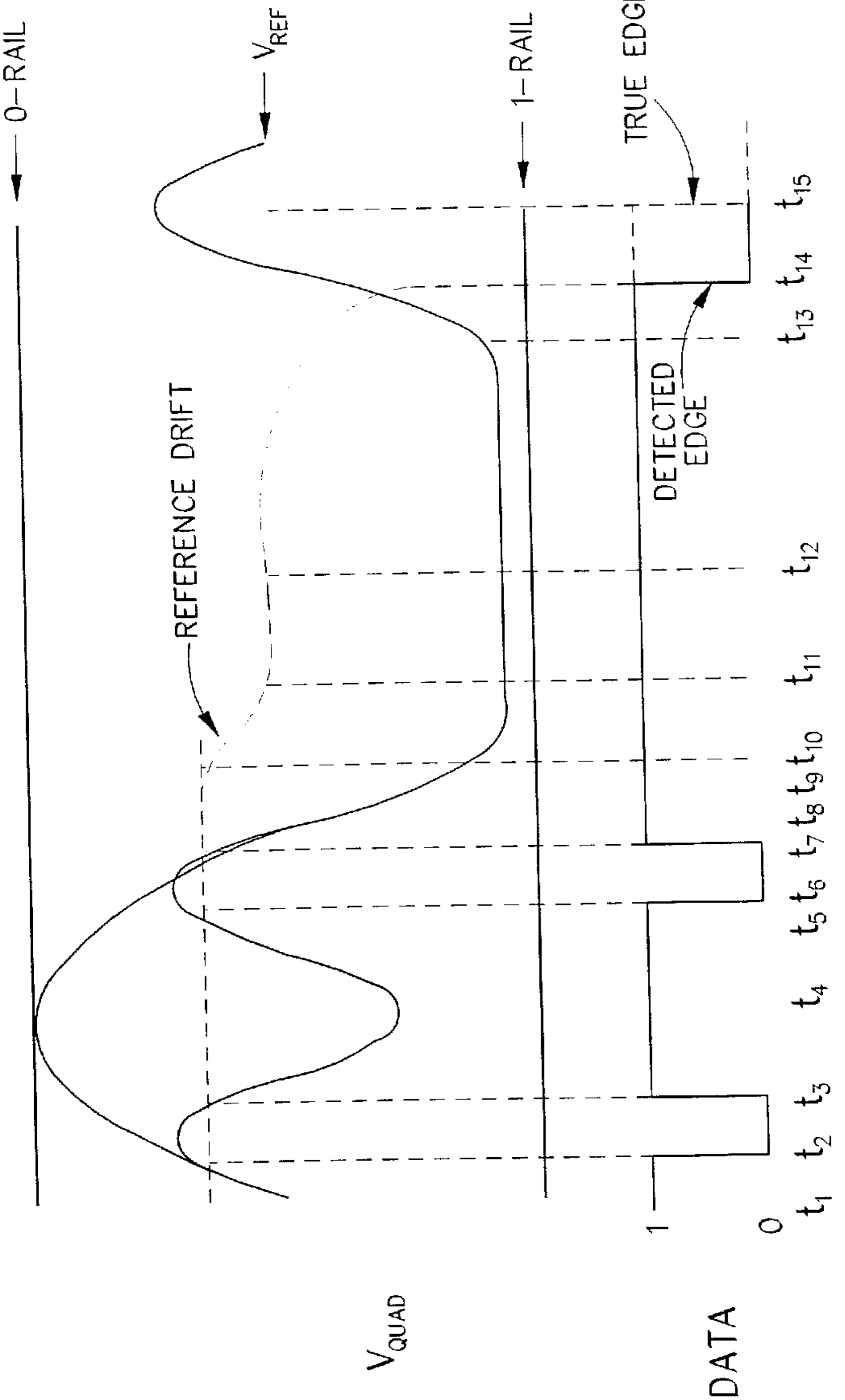
SLICER WITH TRACKING REFERENCE

FIG. 8A



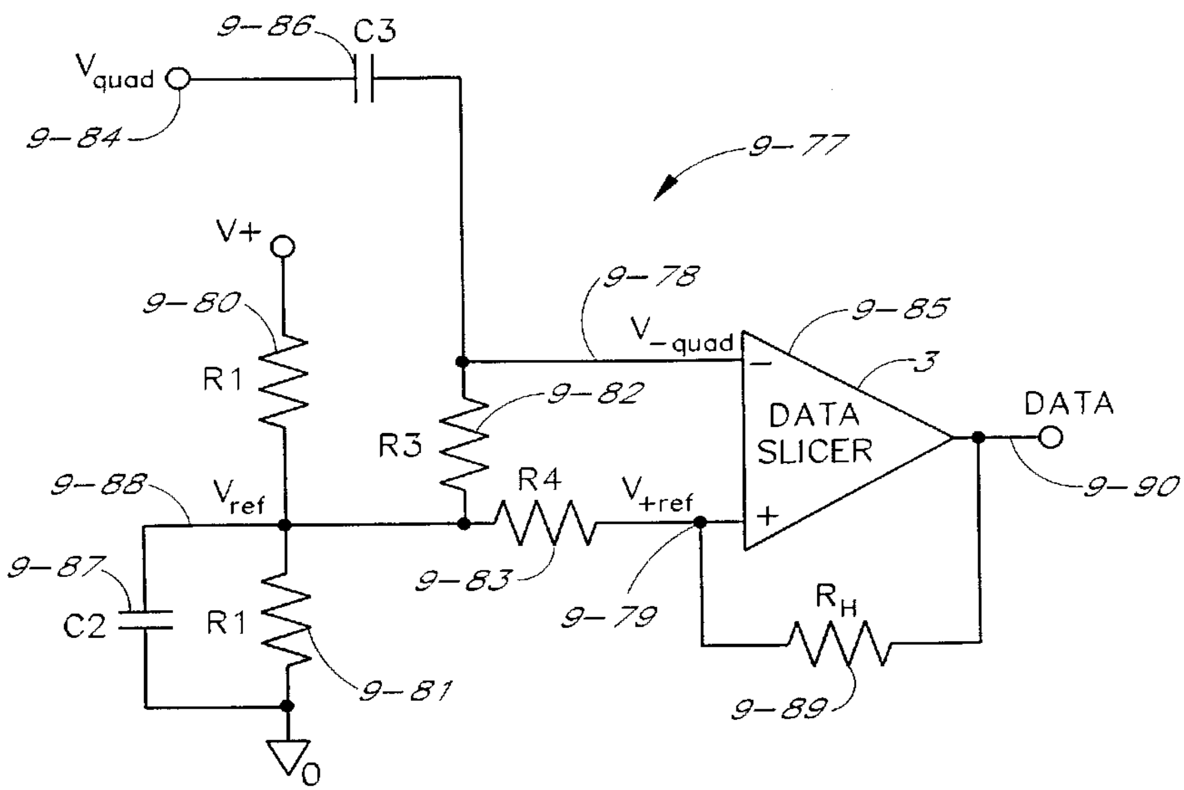
IDEAL OPERATION

FIG. 8B



OPERATION WITH REFERENCE DRIFT

FIG. 8C



AC-COUPLED SIGNAL

FIG. 9A

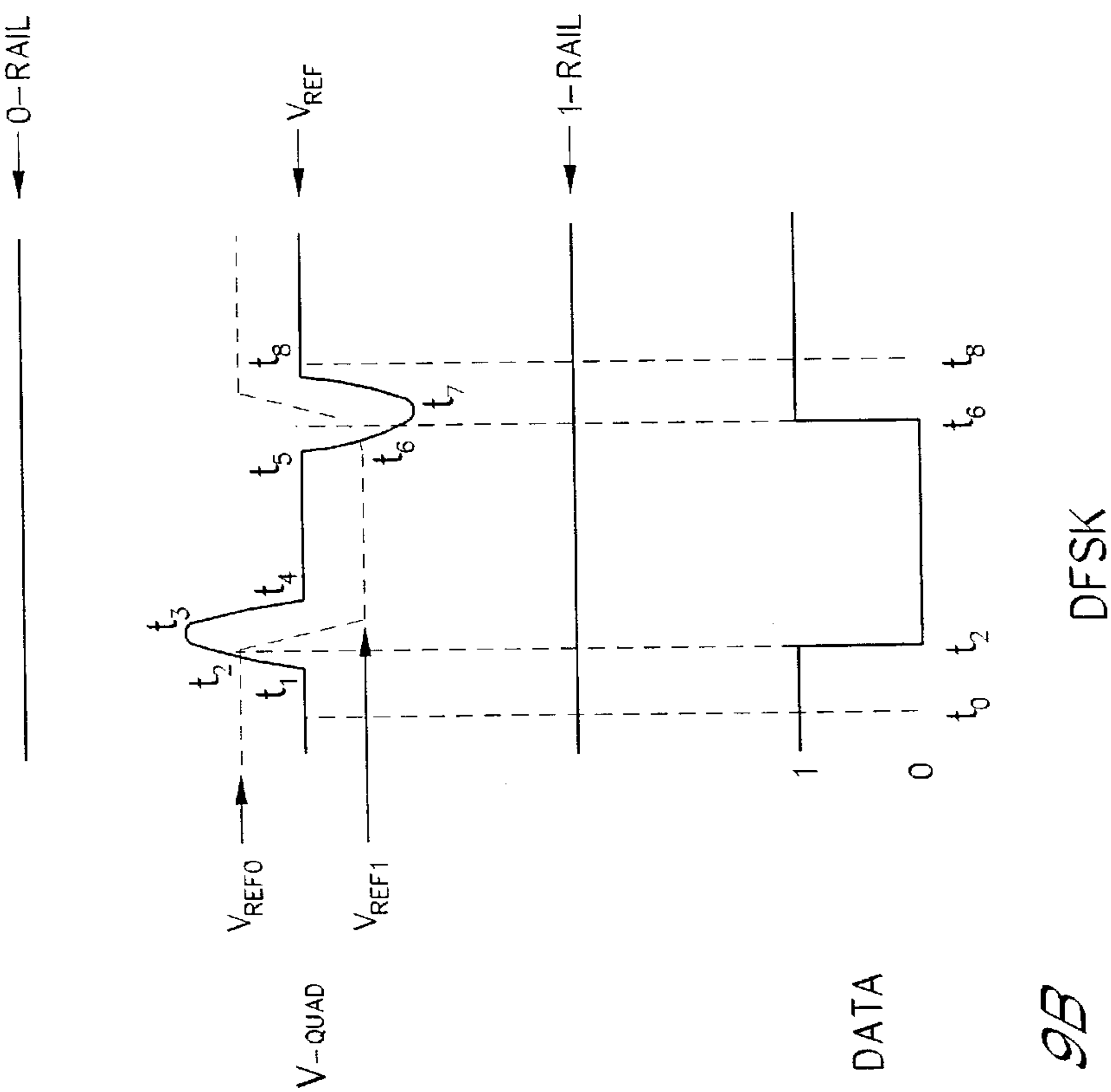
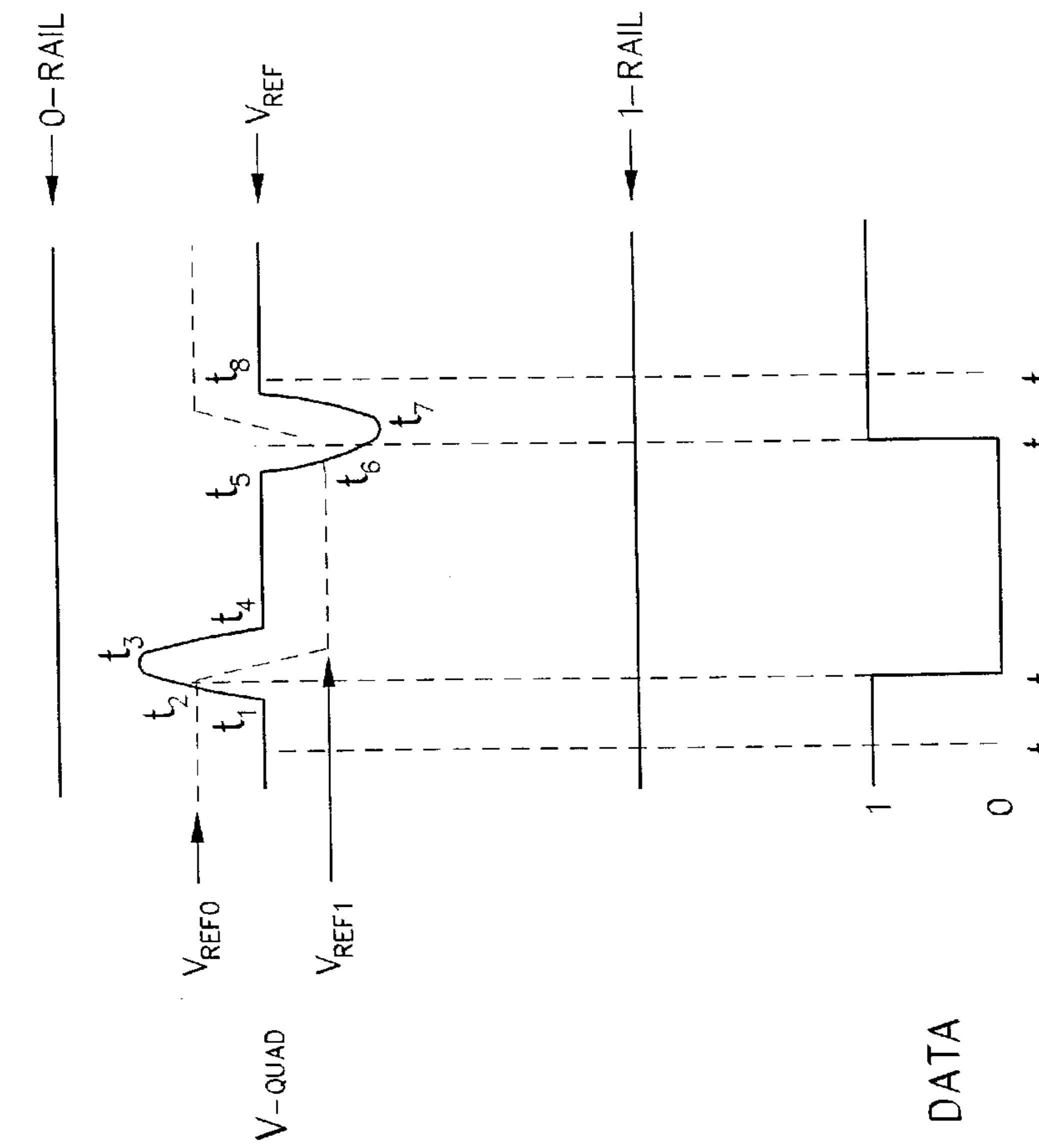

0–RAIL
V_{REF}
1–RAIL
V_{REF0}
V_{REF1}
V_{-QUAD}
DATA
1
0
t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8
DFSK

FIG. 9B



RAILS DRIFT WITH DFSK DETECTOR

FIG. 9C

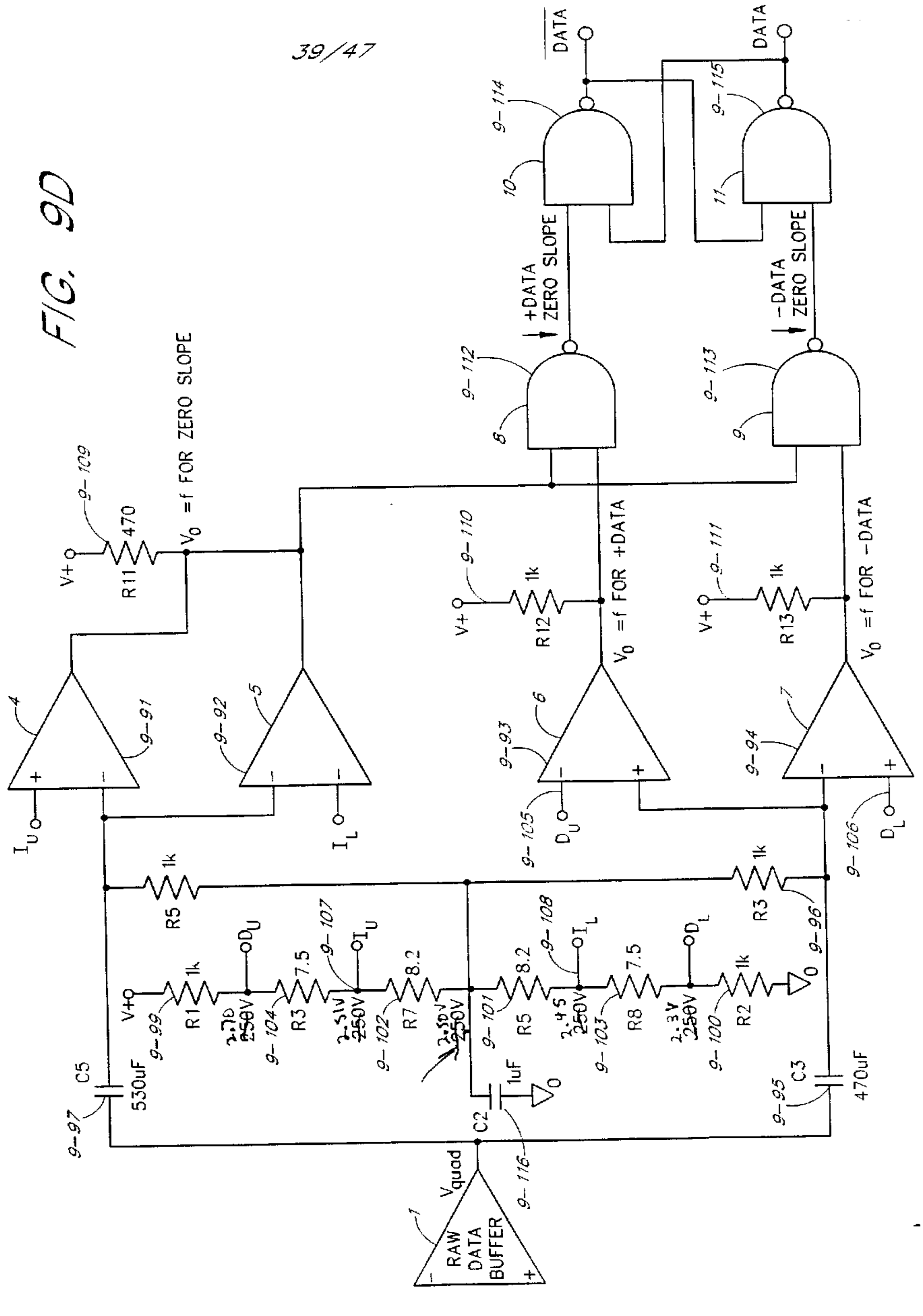

DATA
DATA
9-114
9-115
10
11
+DATA ZERO SLOPE
-DATA ZERO SLOPE
9-112
9-113
8
9
V+
R11
470
9-109
V_0 =f FOR ZERO SLOPE
9-110
R12
1k
V_0 =f FOR +DATA
9-111
R13
1k
V_0 =f FOR -DATA
4
5
6
7
9-91
9-92
9-93
9-94
I_U
I_L
D_U
D_L
9-105
9-106
R5
1k
R3
1k
9-96
R1
1k
R3
7.5
R7
8.2
R5
8.2
R8
7.5
R2
1k
9-99
9-104
9-102
9-101
9-103
9-100
9-107
9-108
C5
530uF
9-97
C2
1uF
9-116
C3
470uF
9-95
V_{quad}
RAW DATA BUFFER
1

FIG. 9D

40/47

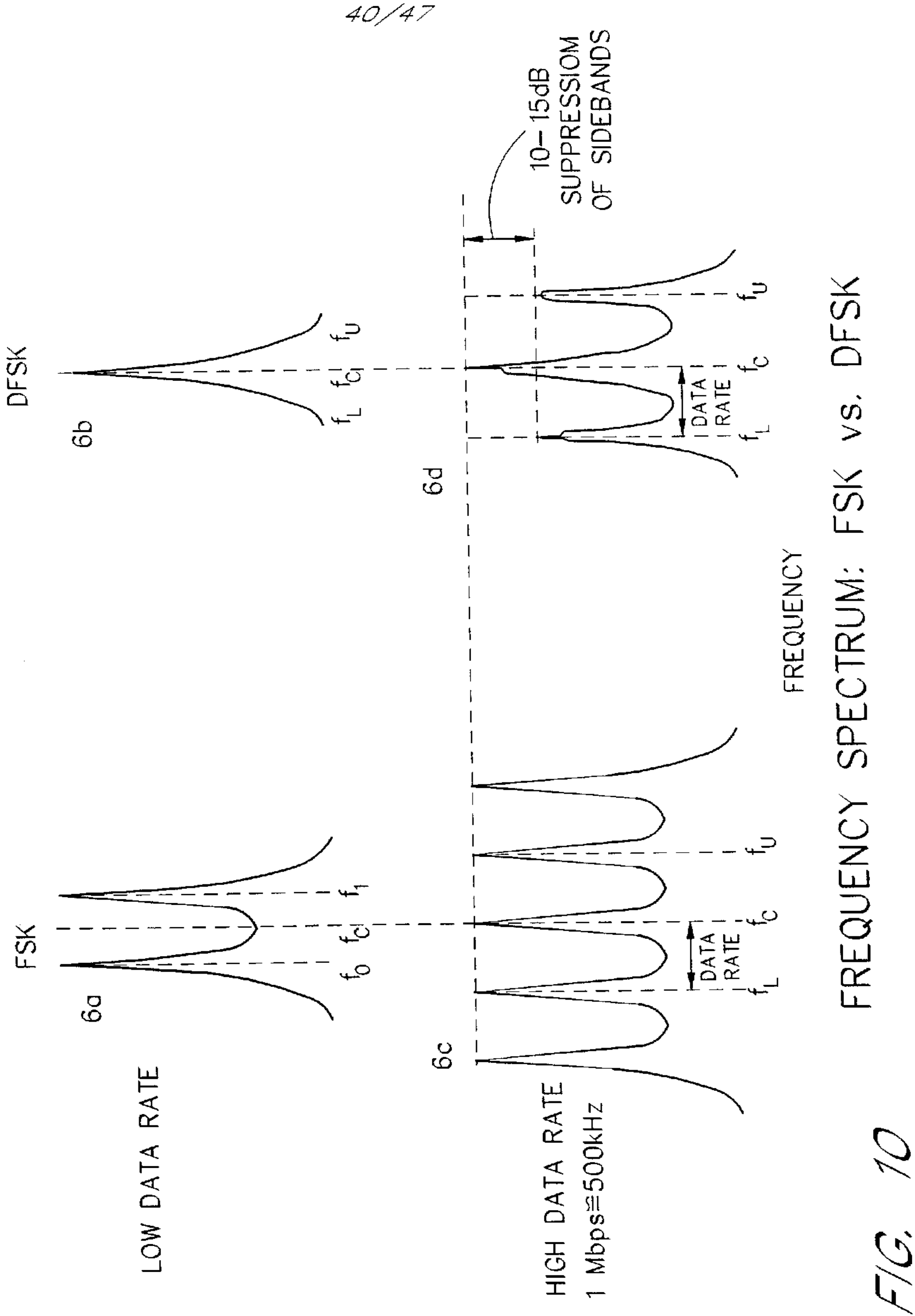
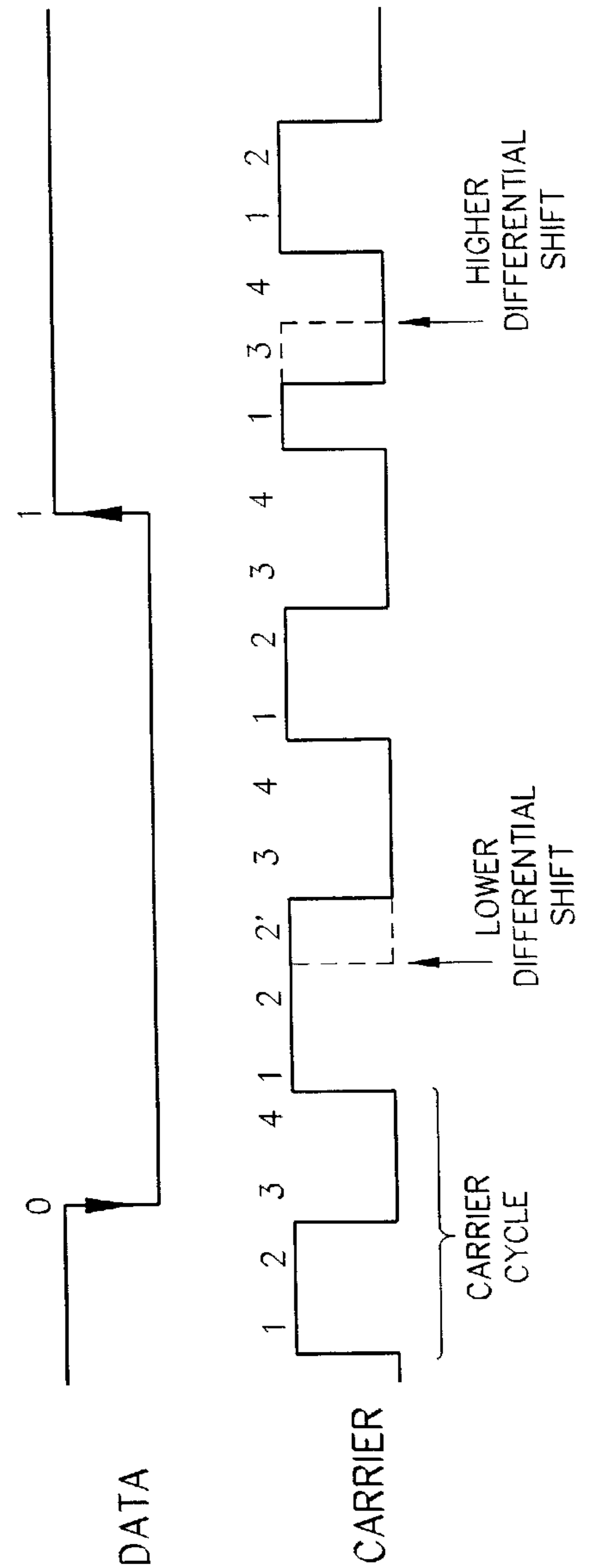

LOW DATA RATE
HIGH DATA RATE
1 Mbps≅500kHz
FSK
DFSK
6a
6b
6c
6d
f_0
f_C
f_1
f_L
f_U
DATA RATE
10–15dB SUPPRESSIOM OF SIDEBANDS
FREQUENCY
FREQUENCY SPECTRUM: FSK vs. DFSK

FIG. 10



DFSK MODULATION

FIG. 11a

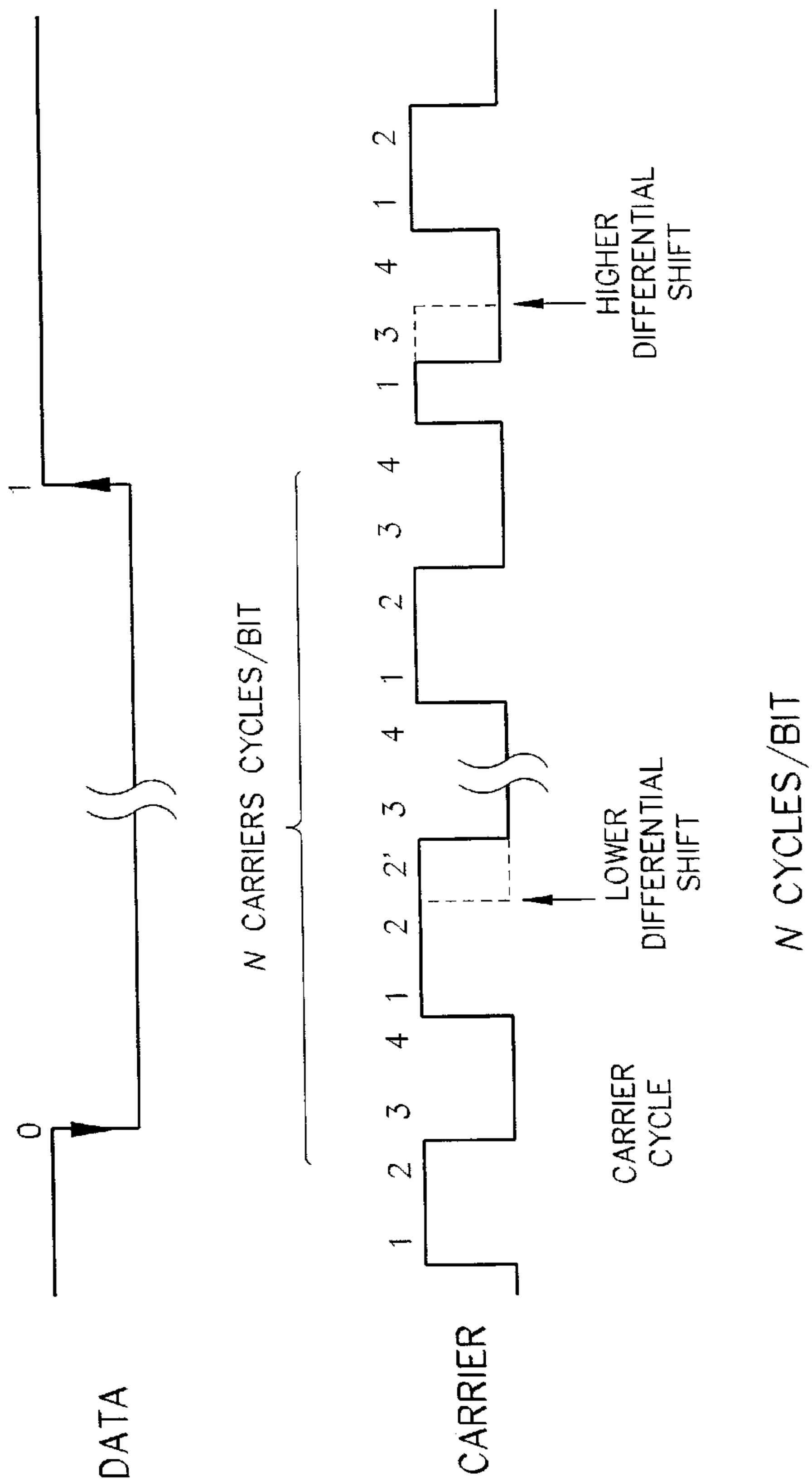
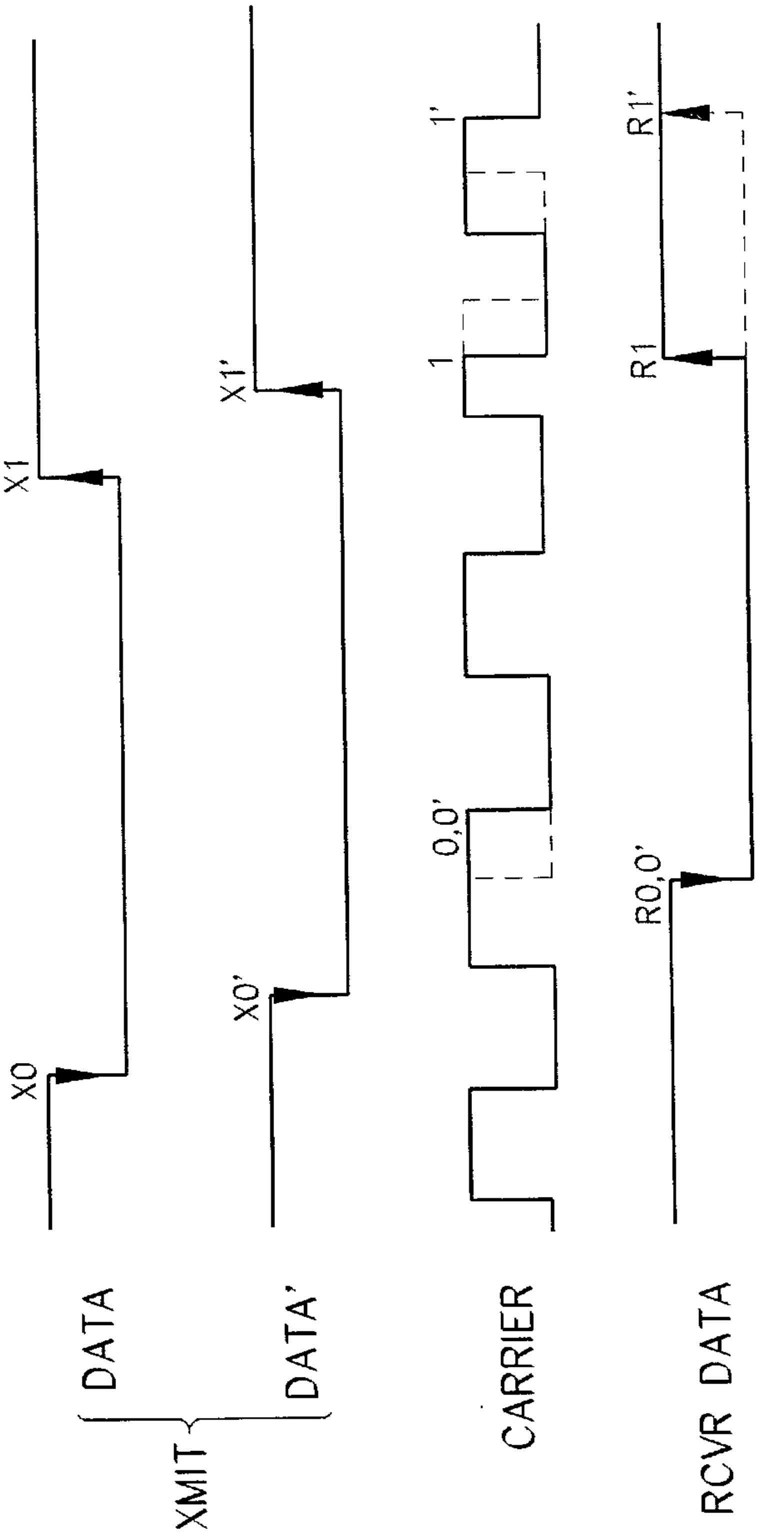

DATA
CARRIER
0
1
N CARRIERS CYCLES/BIT
1 2 3 4 1 2 2' 3 4 1 2 3 4 1 3 4 1 2
CARRIER CYCLE
LOWER DIFFERENTIAL SHIFT
HIGHER DIFFERENTIAL SHIFT
N CYCLES/BIT

FIG. 11B



DATA SYNCHRONIZATION

FIG. 12

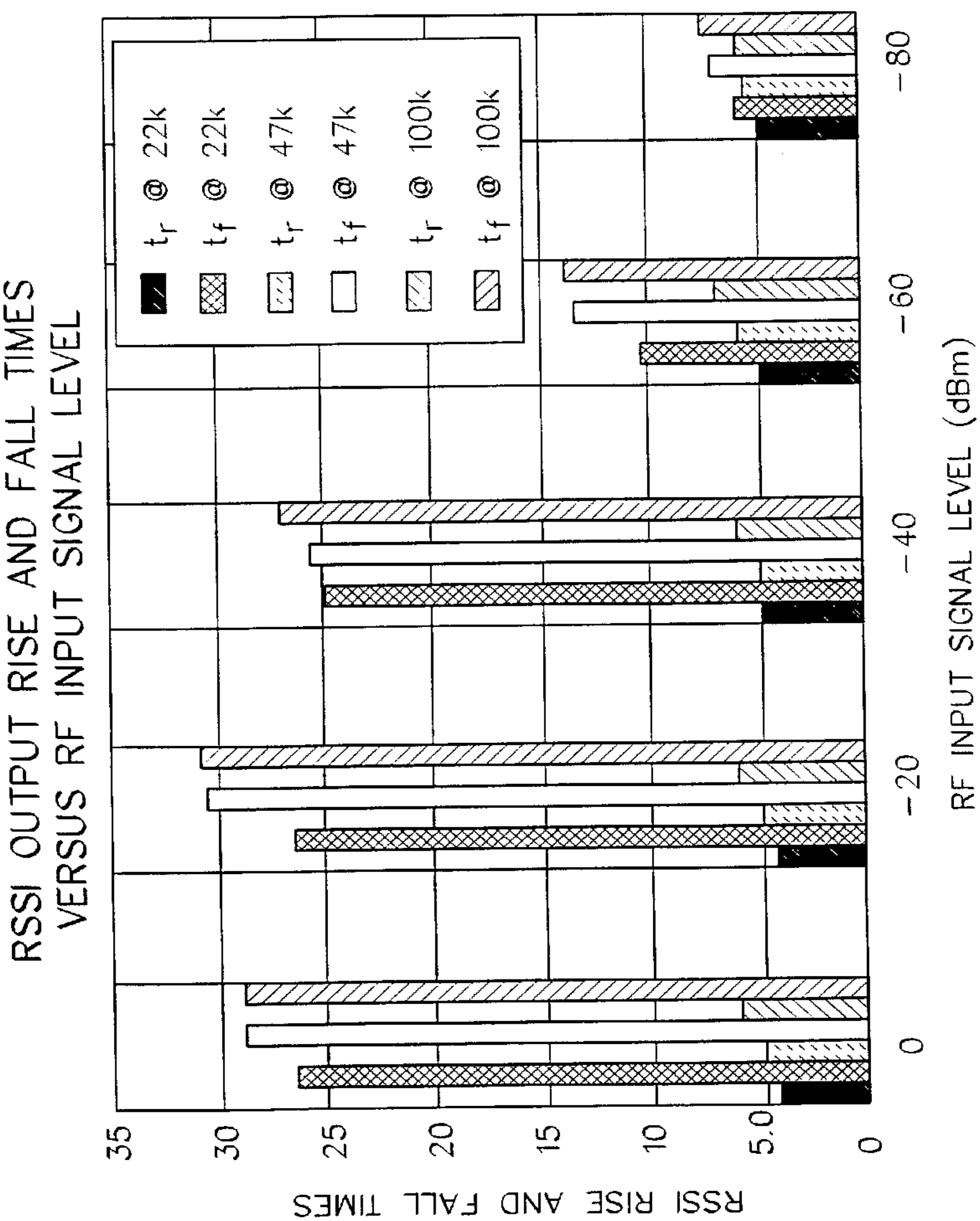
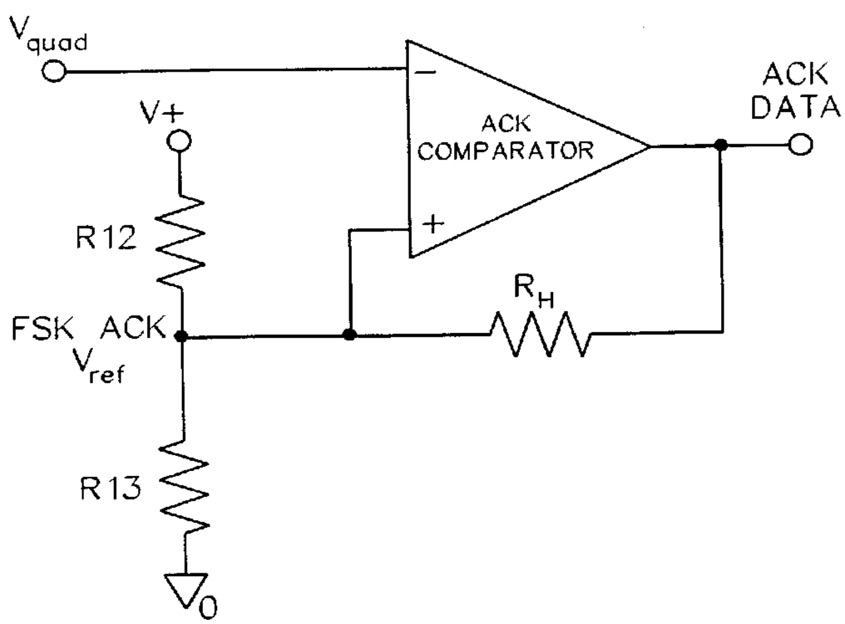

RSSI OUTPUT RISE AND FALL TIMES
VERSUS RF INPUT SIGNAL LEVEL
t_r @ 22k
t_f @ 22k
t_r @ 47k
t_f @ 47k
t_r @ 100k
t_f @ 100k
RSSI RISE AND FALL TIMES
35
30
25
20
15
10
5.0
0
0
−20
−40
−60
−80
RF INPUT SIGNAL LEVEL (dBm)

FIG. 13



ACK COMPARATOR

FIG. 14A

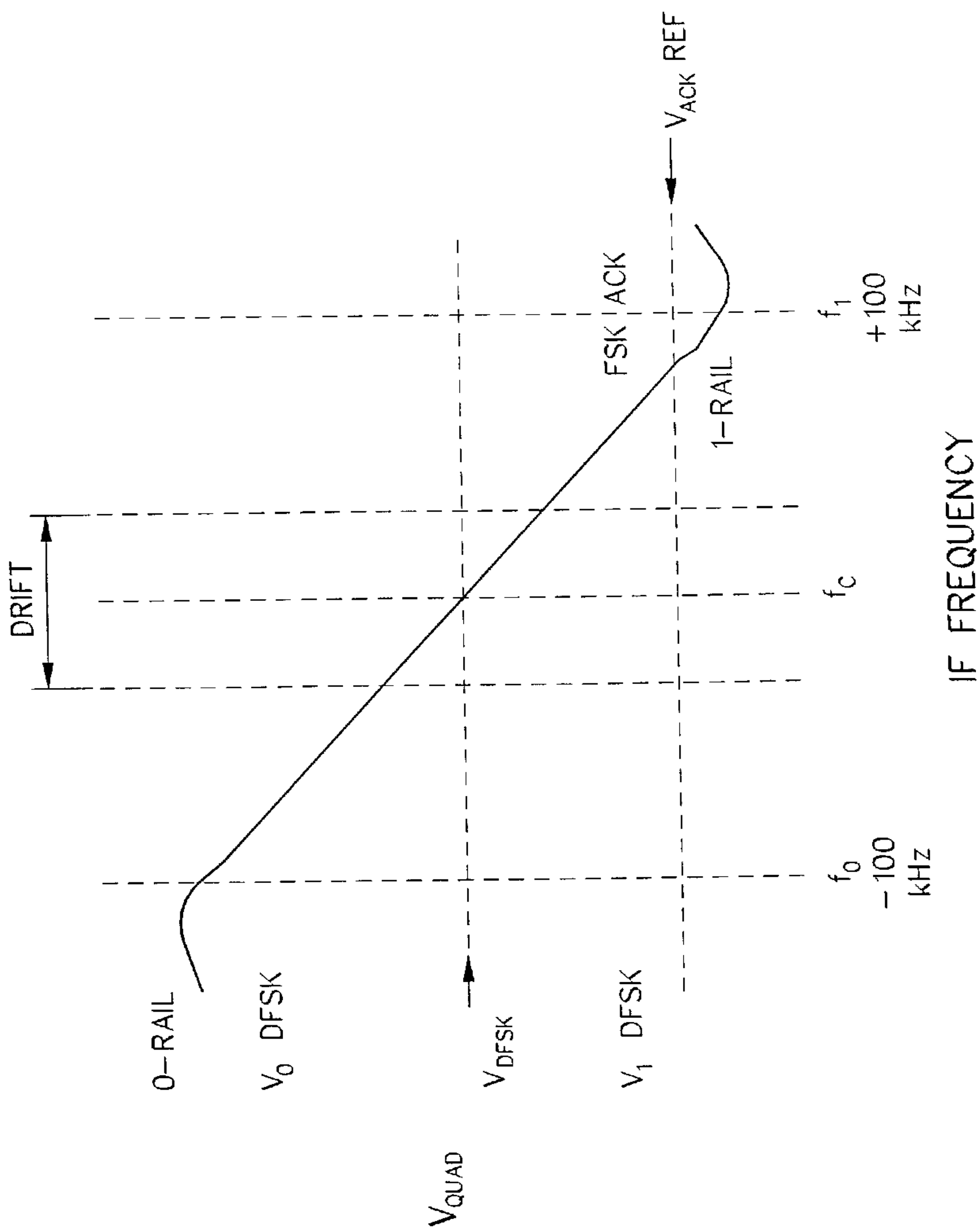

V_QUAD
0–RAIL
V_0 DFSK
V_DFSK
V_1 DFSK
V_ACK REF
DRIFT
FSK ACK
1–RAIL
f_1
+100
kHz
f_C
f_0
–100
kHz
IF FREQUENCY

FIG. 14B

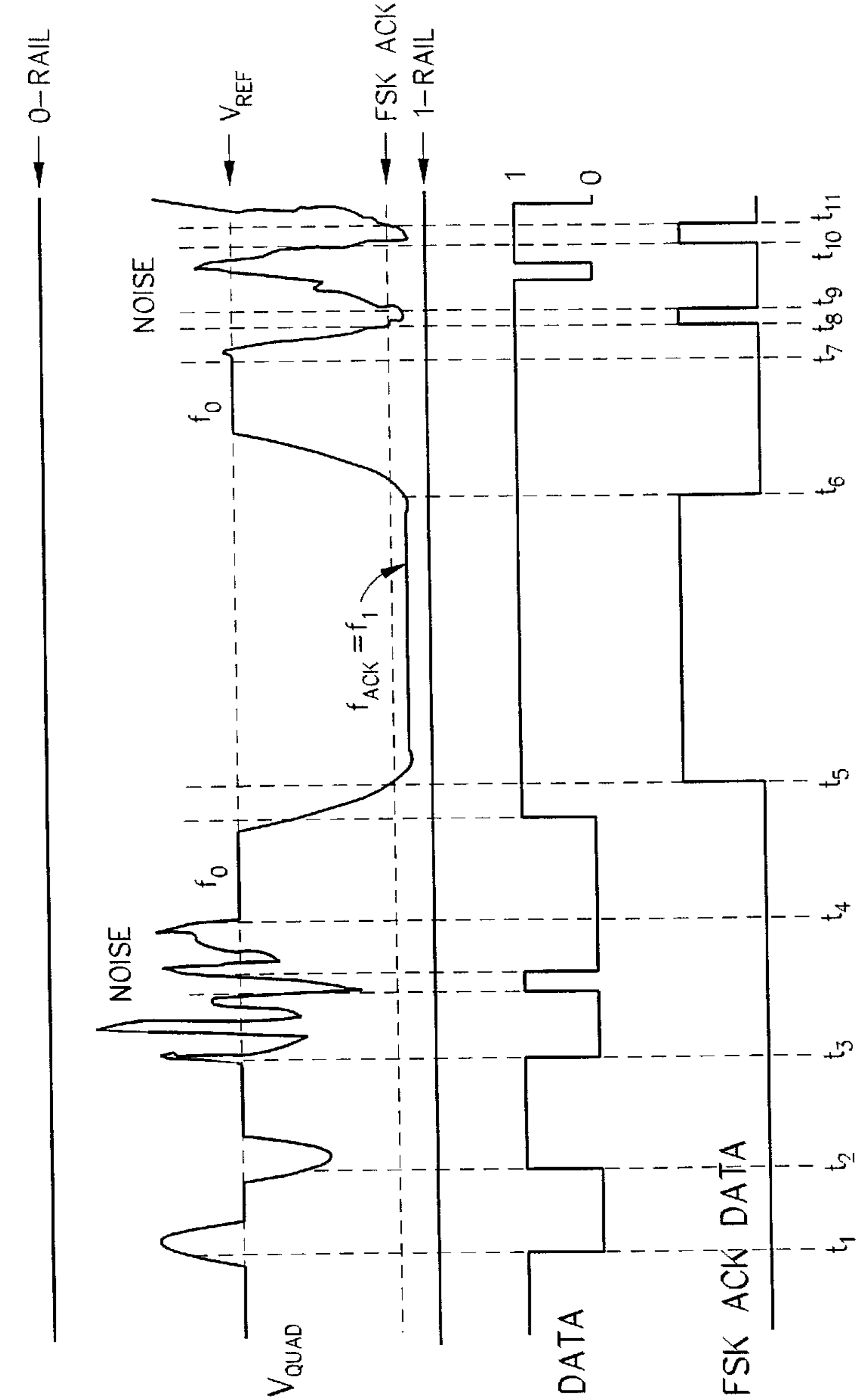

0–RAIL
V_{REF}
FSK ACK REF
1–RAIL
NOISE
f_0
$f_{ACK} = f_1$
NOISE
f_0
1
0
V_{QUAD}
DATA
FSK ACK DATA
t_1
t_2
t_3
t_4
t_5
t_6
t_7 t_8 t_9
t_{10} t_{11}

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/11107

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G01R 31/08; H04H 27/10; H04L 27/10, 27/18, 5/16
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/204, 205, 282, 284; 455/3.3, 403; 375/223, 244, 271, 272, 283, 303, 323, 329,330, 331, 332, 334, 346, 347, 350, 355

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,580,276 A (ANDRUZZI et al) 01 April 1986, Fig. 2, Fig 4, and col. 8, lines 40-68.	1-24
Y	US 4,716,376 A (DAUDELIN) 29 December 1987, col. 1, line 65 to col.2, line 2.	1-24
Y	US 5,305,008 A (TURNER et al) 19 April 1994, col 10, line 47-56.	8
Y	US 4,001,692 A (FENWICK et al) 04 JAN 1977, col. 2, lines 5-7.	9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 AUGUST 1998	01 OCT 1998

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	STEVEN NGUYEN
Facsimile No. (703) 305-3230	Telephone No. (703) 308-8848

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/11107

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

370/204, 205, 282, 284; 455/3.3, 403; 375/223, 244, 271, 272, 283, 303, 323, 329,330, 331, 332, 334, 346, 347, 350, 355